Transparent Current Mirrors Using a-GIZO TFTs: Simulation with RBF Models and Fabrication

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***Abstract*— This paper analyzes transparent two-TFT current mirrors using a-GIZO TFTs with different mirroring ratios. In order to achieve a high mirroring ratio, the output TFT in the circuit employed a fingered structure layout to minimize area and overlap capacitance. The analysis of the current mirrors is performed in three phases. In the first, a radial basis function based (RBF) model is developed using measured data from fabricated TFTs on the same chip. Then, in the second phase, the RBF model is implemented in Verilog-A that is used to simulate two-TFT current mirrors with different mirroring ratios. The simulations are carried out using Cadence spectre simulator. In the third phase, simulation results are validated with the measured response from the fabricated circuits.**

***Keywords*-RBF modeling, a-GIZO TFT analog circuits, Current mirrors.**

I. Introduction

Thin-film transistors (TFTs) are relatively new compared to the silicon integrated circuit (IC) technology. Mainly TFT technologies are intended for large-area, low-cost transparent electronics and display applications such as e-paper [1] and AMLCD [2]. Examples of various TFTs technologies are low temperature poly crystalline silicon (LTPS), a-Si:H, Organic and amorphous semiconductor oxides [3]. LTPS TFT and a-Si:H TFT technologies are not transparent at visible light spectrum, hence they cannot promise transparent electronics. OTFTs and a-Si:H TFTs show poor electron mobility and unstable behavior; however, LTPS TFTs present high mobility and better performance, but its fabrication cost is relatively high. At this phase, TFTs with amorphous semiconductor oxides are gaining significant importance because of their low-cost, low-temperature fabrication and better electrical characteristics. There is an extensive research going on to ensure better performance and low-cost solutions by experimenting different materials and various fabrication techniques. Among various amorphous semiconductor oxides, gallium-indium-zinc-oxide (GIZO) as the TFT active layer is gaining significant importance. The interesting properties associated with the a-GIZO TFT technology are fabrication at room-temperature [4], [5], better optical transparency and the relatively high mobility. These a-GIZO TFT applications are not only confined to displays (AMOLED) [6], but also extended to sensors [7].

The a-GIZO TFT technology is more recent among others. Hence the circuit design reported so far with this technology is not as advanced as with other TFTs. Nevertheless, a shift register [8] and a 6-bit current-steering DAC [9] have been reported with depletion mode n-type a-GIZO TFT. A 23-stage ring oscillator with co-planar enhancement type a-GIZO TFT [10], and a RFID [11] with bottom gate structure have also been reported. Even though a-GIZO TFTs are electrically superior, lack of stable P-type TFTs and built-in library for the active and passive elements with this technology could be the limiting factors for analog circuit design. Analog circuits only with n-type enhancement TFTs promise cost effective solutions as they need one mask less compared to the designs that have both depletion and enhancement type TFTs. Thus, circuits with only n-type enhancement TFTs are reported in this work.

In order to design circuits, accurate device models, which can predict the device behavior in circuit simulations are mandatory. As this a-GIZO TFT technology is very recent, no commercial models are available, nevertheless few articles reported physical modeling [12]. A simple, continuous model with less development time that can accurately predict the small and large signal behavior of the device is a good choice for the new devices like a-GIZO TFT. As artificial neural networks (ANNs) have all the above mentioned properties, they have been employed in this work. A neural model is developed from the measured data of the transistors using radial basis functions (RBF) as this is an universal approximator [13]. Mostly the neural models in circuit simulators are confined to multilayer perceptron (MLP) networks [14] [15], [16], [17]. Even though the RBF network needs more neurons to promise good accuracy compared to MLP networks, RBF training and its implementation in

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analog HDL tools are much simpler as the RBF network does not require pre and post processing. The developed RBF model is implemented in Verilog-A, to simulate the circuits with commercial simulators like Cadence Spectre. To the authors knowledge, these are the first RBF neural models that are used for circuit simulations.

Current mirrors are important functional blocks in analog circuit design, which are basically used to provide bias current for the circuits or serve as an active load. Current mirrors with a-Si:H TFTs [18] and ZTO TFTs [19] are reported, where the ZTO TFT has an average mobility of $\sim 7\,\mathrm{cm}^2$/V.s for 3:1 composition with SiO_2 gate dielectric and aluminum source-drain contacts. In this work, simple two-TFT current mirrors with different mirroring ratios, using n-type enhancement a-GIZO TFTs are characterized. At higher mirroring ratio, the output transistor employs a fingered-structured layout, which results in faster circuit operation and less area. However this paper is confined to only static behavior characterization of the TFT circuits. All the individual isolated active and passive elements are also fabricated on the same chip. From the measured characteristics of these isolated TFTs, RBF model is developed and then this model is used to simulate the two-TFT current mirror circuits. The simulation results are validated with the real circuits response, to prove the ANN modeling ability as well as current mirroring capability of the a-GIZO TFTs.

The rest of the paper is organized as follows. Section II gives a brief introduction to modeling, section III demonstrates current mirrors fabrication details and static behavior characterization. Section IV shows the results and discussion. Finally section V presents the conclusions.

II. RBF Modeling

A typical radial basis function (RBF) network consists of a single input, hidden and output layers as shown in Fig. 1. This network is meant to model the a-GIZO TFT drain current (I_D) in terms of bias voltages (V_{DS}, V_{GS}) and width (W) of the transistor. Each layer in the network has

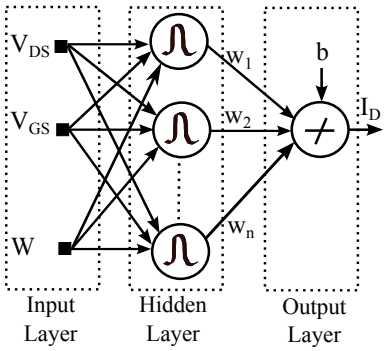


Figure 1: RBF network topology to model drain current (I_D) of TFT in terms of bias voltages (V_{DS}, V_{GS}) and transistor width (W)

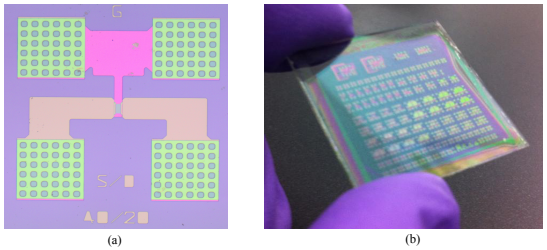
a different functionality. The input layer contains sensory nodes, to which the input patterns are applied. The hidden-layer neurons contain radial-basis functions. This layer transforms the input space into a non-linear hidden space. Mostly the hidden-space has higher dimensionality. In this work, Gaussian functions have been used as the basis functions. Hence the i^{th} neuron output (y_i) in the hidden layer is expressed by,

$$y_i = exp^{-\frac{\|(x-t_i)\|}{2\sigma^2}}. \quad (1)$$

where x is the input sample, t_i is the center and σ is the spread of the Gaussian function for the i^{th} neuron in the hidden layer. During the training phase, proper value of σ should be selected to avoid either highly localized or too flat response from the hidden layer neurons. The neurons at the output layer are linear in nature. They perform a weighted summation of the outputs from the hidden layer neurons to the connecting weights between hidden and output layer. The output layer provides the network response for the activation samples [20].

III. Method : Simulation, Device fabrication and Characterization

The two-TFT current mirrors with different mirroring ratios and isolated active and passive components are fabricated on the same transparent substrate. The fabricated TFT and the complete chip are shown in Fig. 2. One has to notice



(a) (b)

Figure 2: (a) Fabricated TFT with width (W) = 40 μm and Length (L) = 20 μm (b) A chip containing all the circuits and the isolated active and passive elements

that these a-GIZO TFTs do not exhibit body effect unlike MOSFETs, since the bulk is an insulator. For these devices, highly conductive and transparent Indium-Zinc oxide (IZO) source-drain and gate electrodes are used, together with the GIZO semiconductor. The dielectric is a multilayer/multi component structure (SiO_2/Ta_2O_5-SiO_2/SiO_2). All these layers are deposited by rf magnetron sputtering at room temperature. More details about the fabrication process can be found in [21], [22]. On the top of this structure, a SU8 layer was spin-coated to act as a passivation layer [23]. The TFTs employed in this work have staggered bottom gate structure and they exhibit a mobility of $\sim 20\,\mathrm{cm}^2$/V.s.

Current Mirrors with two TFTs

The schematic and fabricated two-TFT current mirrors are shown in Fig. 3 and Fig. 4 respectively. The fabricated circuits employ passive resistors. As a matter of fact, models

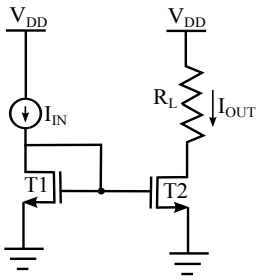
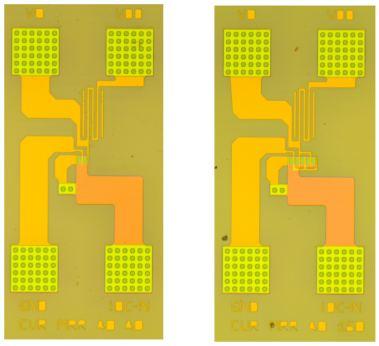


Figure 3: Schematic of current mirrors with two TFTs



(a) (b)

Figure 4: Fabricated current mirrors with two TFTs with (a) W_2 = 40 μm (b) W_2 = 160 μm

for passive elements are not available with this technology. Hence the isolated resistor is also fabricated on the same chip for its electrical characterization. The resistor layout is shown in Fig. 5. It is fabricated with IZO material, which is also used for source/drain and gate electrodes of the TFT. Interconnections between circuit elements and pads are also carried out by the same material.

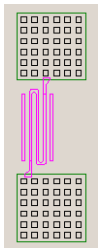
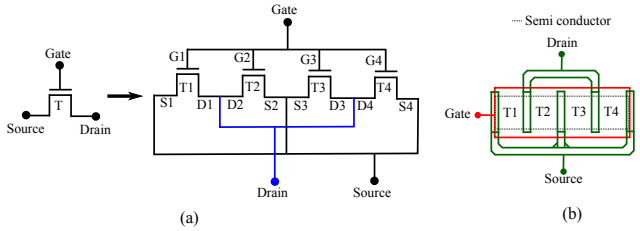


Figure 5: Resistor layout

In Fig. 4(a), TFTs T1 and T2 have a width (W_1 = W_2) of 40 μm. In Fig. 4(b) TFTs T1 and T2 have widths of W_1 = 40 μm and W_2 = 160 μm respectively. All the transistors have the same length of 20 μm. When the TFT width is 160 μm, the design followed a layout that promises less area and faster operation, i.e. a fingered structure is used. This TFT is expressed as a parallel connection of four TFTs with 40 μm width as shown in Fig. 6.

Considering FET I/V characteristics, an approximate behavior of the a-GIZO TFT in saturation region for the drain current (I_{DS}) can be expressed as (2).



(a) (b)

Figure 6: Wider TFT (a) Equivalent representation (b) Layout for W_T = W_{T1} + W_{T2} + W_{T3} + W_{T4} and same length

$$I_{DS} \approx K' \frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tag{2}$$

where K' is constant related to the fabrication process, $\frac{W}{L}$ is the aspect ratio, V_T is the threshold voltage, and λ is the channel length modulation parameter of the TFT. As the TFTs under consideration have the same length, Fig. 3a results in

$$\frac{I_{DS2}}{I_{DS1}} = \frac{I_{OUT}}{I_{IN}} = \frac{W2(V_{GS} - V_{T2})^2(1 + \lambda V_{DS2})}{W1(V_{GS} - V_{T1})^2(1 + \lambda V_{DS1})}. \tag{3}$$

If devices are matched and the channel length modulation is neglected (due to the long length of the TFTs) (3) can be approximated to

$$\frac{I_{OUT}}{I_{IN}} \approx \frac{W2}{W1}. \tag{4}$$

IV. Results

In order to train the network, measured data from TFTs that are on the same chip with widths 40 μm, 160 μm and 320 μm were used. All TFTs have the same length (20 μm). The drain current (I_{DS}) is measured by sweeping bias voltages (V_{GS} and V_{DS}). For the RBF model, inputs are transistor widths and bias voltages, where V_{GS} and V_{DS} are ranging from 0 to 10 V and 0 to 15 V in steps of 1 V. MATLAB 2011b is used to train the RBF network. Its performance in terms of mean square error (MSE) for different number of neurons and spreads of the Gausssian functions are reported in Table. I. These results show that, as the spread increases, the MSE reduces, especially, for less number of neurons. If the spread is too high then the network cannot learn from the training samples since all neurons respond in the same fashion to the inputs.

In order to increase the model accuracy, a separate network is developed for each TFT. The RBF networks are implemented in Verilog-A for circuit simulations. This Verilog-A model response for the testing data (which is not used in the training phase) is obtained from the DC analysis in Cadence environment. Then these results are validated with the measured data as shown in Fig. 7 and Fig. 8 that demonstrates the generalization ability of the RBF model.

The electrical behavior of the isolated resistor is characterized by sweeping the voltage across its terminals in forward and backward directions. This type of characterization tests

Table I: RBF NETWORK PERFORMANCE

Spread	No.of Neurons	MSE	Epochs
2	25	2.46e-10	25
2	50	8.60e-11	50
2	75	4.38e-11	75
2	100	3.32e-11	100
2	150	2.89e-11	150
2	200	2.65e-11	200
4	25	6.34e-11	25
4	50	3.40e-11	50
4	75	3.24e-11	75
4	100	2.56e-11	100
4	150	2.52e-11	150
4	200	2.51e-11	200
6	25	4.17e-11	25
6	50	2.92e-11	50
6	75	2.53e-11	75
6	100	2.53e-11	100
6	150	2.53e-11	150
6	200	2.53e-11	200

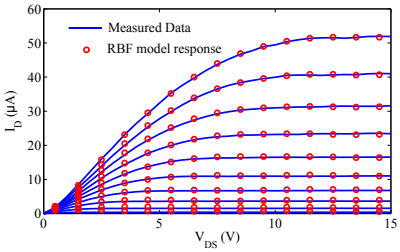


Figure 7: Verilog-A RBF model response for : W = 40 μm, V_{DS} ranging from 0.5 to 14.5 V in steps of 1 V and V_{GS} ranging from 0.5 to 9.5 V in steps of 1 V

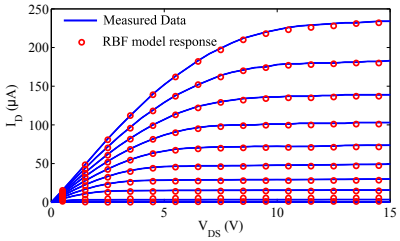


Figure 8: Verilog-A RBF model response for : W = 160 μm, V_{DS} ranging from 0.5 to 14.5 V in steps of 1 V and V_{GS} ranging from 0.5 to 9.5 V in steps of 1 V

the hysteresis behavior of the resistor. The electrical behavior of the resistor is shown in Fig. 9. This response reveals a good linear relationship between voltage and current. Its value is found to be 2.25 KΩ.

In order to simulate the circuit shown in Fig. 3, RBF Verilog-A models are used for the TFTs. The current mirror load (R_L) is 2.25 KΩ and the power supply (V_{DD}) is 10 V. Then these simulation results are validated with the measured circuit response. During the real circuit measurements

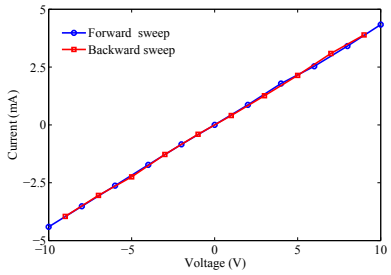


Figure 9: Resistor characterization

also the same V_{DD} of 10 V is used. Expected behavior of current mirrors, simulation results and the real circuits response are shown in Fig. 10. From these results, minor mismatches between the simulation, measured and expected behavior can be noticed. The probable causes are the leakage current, modeling error, non-idealities related with noise due to the IZO contacts while obtaining TFT measured data for RBF model and the geometry in the actual device is not exactly the same as predicted by the mask design. However, the shift between actual measured results and predicted by simulation does not exceed 5 percent.

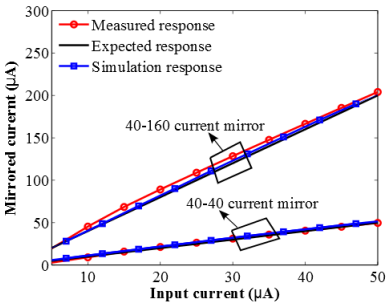


Figure 10: Two-TFT current mirrors response with different mirroring ratios: from circuit simulations, measured and expected behavior

V. Conclusions

A RBF model is developed from the measured data of the TFTs, which are on the same chip as the circuits. Then it is implemented in Verilog-A for circuit simulations. The isolated passive resistor on the same chip is also characterized. The schematics of the fabricated circuits are simulated using the Cadence Spectre simulator. The simulation results are validated with the fabricated circuit response, and they are in good agreement with the expected behavior.

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