

# Design of a High Efficiency GaN-HEMT RF Power Amplifier

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**Abstract**—This paper presents the design and implementation of a GaN-HEMT, class-J power amplifier suitable for cognitive radio transceivers, i. e., which presents high-efficiency and wideband characteristics, being these maintained for large load variations. Simulation results are presented which show large-signal measurement results of 30 dB gain with 60%-76% power-added efficiency (PAE) over a band of 1.3-2.3 GHz. Adaptivity to load changes is being developed to ensure PAE above 70% for large load variations.

**Index Terms**—GaN HEMT, Class-J, Power amplifier, Cognitive Radio

## I. INTRODUCTION

THE next generation of wireless communication devices must achieve Gigabit data rates and low power consumption by means of making more efficient use of the radio frequency spectrum and taking advantage of device interoperability. This has motivated the development of cognitive radio systems, i. e., radios whose transmission parameters can be adapted according to their interaction with the operating environment.

Cognitive radio (CR) architectures are being developed aiming at providing high-performance platforms supporting radio frequency (RF) spectrum scanning capability, adaptive frequency bandwidth transceivers, and a software-defined radio (SDR) modem capable of supporting multi-standard and multi-band operation, different waveforms and protocols. SDR implementations can be modulation flexible in a certain frequency range, such as it is required with UMTS and IEEE 802.16, or modulation and frequency flexible [10]. The last one provides more flexibility on the use of the available spectrum or dynamic adaptation to different wireless networks. On the other hand, frequency agility approaches are more demanding concerning the design of the radio front-end, namely in terms of matching networks bandwidth, as a trade-off between efficiency and bandwidth has to be made, implying thus a suboptimal solution.

Besides flexible functionality, the CR and SDR developments seek also performances for green technology, i. e., lower power, after replacing power hungry analogue by digital implementations, demanding in particular RF power amplifiers (PA) capable of presenting high efficiency over a large frequency bandwidth.

These new technologies are also opening new doors within the healthcare applications, both for data communication purposes [11], as well as, for application specific systems such as using IR-UWB for non-invasive imaging of different physiological parameters, non-ionizing cancer detection and treatment procedures, without the restricted use of conventional X-ray procedure for screening, and fracture healing [12]–[14], as well as, remote patient monitoring with relatively cheaper equipment cost [1]. The remote monitoring of vital signals, such as heartbeat or breathing rate, outside conventional clinical settings (e.g. at home), may increase accessibility to and decrease healthcare delivery costs [2].

The development of cognitive radio transceivers for all these applications raises severe challenges to the PA design, as this is the most critical component since its performance strongly influences the overall system features in terms of bandwidth, output power, efficiency, and operating temperature. The design of wideband PAs which operate in multiple frequency bands while maintaining high efficiency, has gained significant attention from research and industries. PAs are classified into several classes based on the conduction angle of the drain current and further divided into linear and non-linear. The linear PAs present good linearity but poor efficiency, whereas the non-linear PAs have the advantage of higher efficiency at the cost of poor linearity [3].

In 2006 [3] and 2009 [4], S. C. Cripps proposed the Class-J amplifier that provides good efficiency and linearity, similarly to AB and B classes amplifiers, across a broad frequency range due to the absence of the resonant impedance condition, such as short-circuit or open-circuit. The Class-J PA uses the second harmonic tuning to reduce the DC power dissipation and to increase power efficiency.

The most popular technique that is used to design broadband amplifiers is the distributed or travelling-wave amplifier approach [5]. In this case, a linear design method is used that ensures linearity, flat gain, and high return loss over the whole band.

In this paper, we present the design of a class J PA which shows high-efficiency over a wide bandwidth. The design is based on a source-pull/load-pull simulation approach together with a detailed method for the design of suitable input and output matching networks. An analysis of the impact of each component tolerance on the overall PA efficiency and linearity

performance obtained after Monte Carlos (MC) simulations, allowed to identify the most critical components for the development of self calibration and self tuning methodologies.

## II. AMPLIFIER DESIGN

### A. Fundamental principles

The Class-J key design manoeuvre is to shift the phasing of the voltage and current waveforms, without changing their shape, such that the second harmonic voltage and current components are in quadrature phase [3]. The design has potential to maintain high power and efficiency over a large bandwidth for both inductive and capacitive second harmonic terminations. This can be obtained using the conventional Class-B operation which presents a resistive load at fundamental frequency and short circuits all harmonic frequencies. However, for Class-J the resistive plus reactive load presented at the fundamental frequency and the capacitive termination for the second harmonic boosts the voltage amplitude while maintaining the same efficiency as the Class-B operation. The mathematical expressions to obtain the Class-J operation from the Class B continuous mode are given as in [3].

The Class-B transistor drain voltage wave ( $V_B$ ) shows a DC offset as represented in equation  $V_B = V_{pk} * \sin(\theta) + V_{dc}$  where  $V_B$  is the sine wave with DC offset and whose peak voltage  $V_{pk}$  exactly equals to the DC offset at the point before the amplifier compresses. In that case we can rewrite,

$$V_B = V_{dc} * (1 + \sin(\theta)) \quad (1)$$

The Class J transistor drain voltage waveform ( $V_J$ ) is obtained from,

$$V_J = V_B * (1 + \cos(\theta)) \quad (2)$$

$$V_J = V_{DC} * (1 + \sin(\theta) + \cos(\theta) + \sin(\theta)\cos(\theta))$$

$$\sin(\theta)\cos(\theta) = \frac{1}{2}\sin(2\theta)$$

The  $\sin(2\theta)$  term shows that the second harmonic adds in phase to boost the fundamental.

In general terms, the family of voltage waveforms is obtained from equation

$$V_J = V_B * (1 + \alpha \cdot \cos(\theta)) \quad -1 \leq \alpha \leq 1 \quad (3)$$

where  $\alpha = 1$  corresponds to the Class J case and  $\alpha = 0$  to the Class B case. The Class-J voltage and current waveforms obtained from these equations are presented in figure 1.

### B. Design methodology

The methodology to design a PA operating in Class-J mode is as follows.

- 1) The key feature of the task is to design the harmonic and fundamental matching networks so that the load pulling and source pulling techniques are performed to obtain the optimum source and load impedances

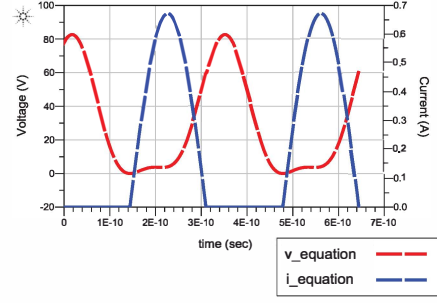


Fig. 1: Class-J drain current and voltage waveforms.

at fundamental and 2nd harmonic to achieve high efficiency.

- 2) The suitable matching networks are designed in order to realize the obtained impedances at the device input and output terminals.
- 3) Verification of intrinsic current and voltage waveforms in order to reduce the power dissipation and optimize the power added efficiency (PAE).
- 4) The robustness of the design is analysed after Monte Carlo (MC) and Electromagnetic (EM) simulations. The EM simulation is performed on the transmission lines to ensure the synthesis of the input and output matching networks, being MC simulation used to analyse the uncertainty introduced by the tolerance of the lumped components.

The complete schematic of the design is shown in figure 2. The dynamic range of the amplifier is increased with the addition of a pre-amplifier stage.

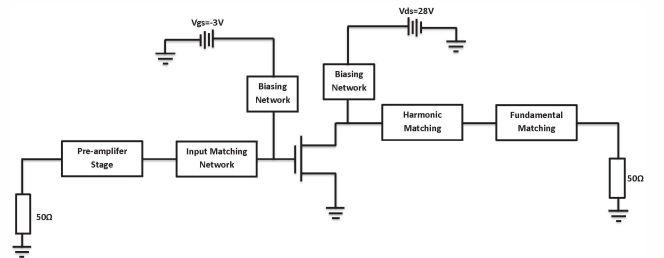


Fig. 2: Block diagram of the Class-J PA.

### C. Device model

A Cree CGH40010 [6] Gallium-Nitride (GaN) high-electron-mobility transistor (HEMT) is used in the present PA design. From the I-V characteristics of the CGH40010 ADS model the biasing condition is determined based on the class of operation. A drain bias voltage of 28 V is used and the gate bias voltage is chosen as -3 V, which is close to the cut-off region for Class-J operation.

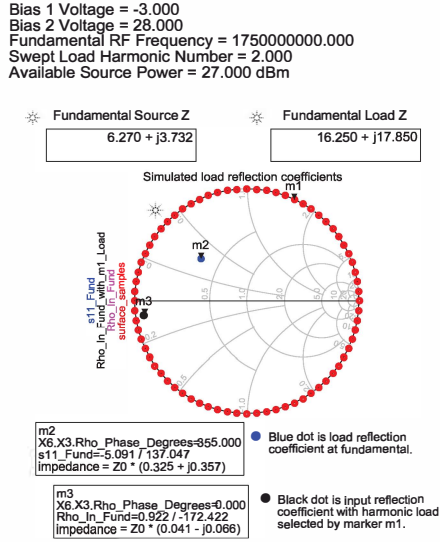


Fig. 3: Load and source impedance contour.

#### D. Load-pulling analysis

A load-pull simulation is conducted on the GaN transistor in order to obtain a more accurate load and source impedance than using the packaged transistor model [7]. The power performance and the efficiency can be analysed from the load pulling measurements. The load impedance is pulled over a range with the load tuner, being the power delivered and the efficiency analysed from the respective contours. The same is repeated for the source side.

The intrinsic source and load impedances at the mid bandwidth (1.75 GHz) are not provided in the manufacturer data-sheet, so the load pulling technique is used, being the source and load impedances swept to conjugate match with the transistor intrinsic impedances at fundamental and second harmonic, to obtain the highest PAE and gain with maximum RF input drive.

Figure 3 shows the load contour plot obtained with a load impedance value of  $16.25 + j17.85$  and source impedance value of  $6.27 + j3.73$ . With these optimal impedances a 83.4% PAE is obtained and a load harmonic sweep is performed where the phase of the second harmonic load is swept (red dots in the figure 3) to analyse how the reflection coefficient of the 2nd harmonic affects the overall PAE. That evolution presented in figure 4 shows that a significant variation occurs. Both input and output matching networks were then designed to directly match these impedances.

For Class-J analysis, an input signal frequency of 1.75 GHz with power of + 27 dBm is applied while the transistor is biased at -3V  $V_{gs}$  and 28 V  $V_{ds}$ . These input conditions were consistently used in the design for the overall amplifier comparison.

#### E. Matching network

The proper input and output matching networks will provide the maximum power delivery to the load and increase the

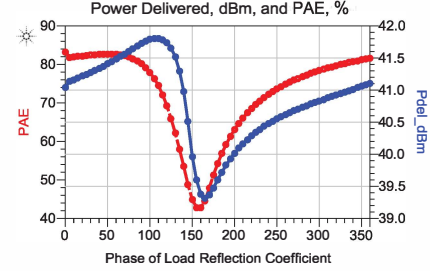


Fig. 4: Output delivered power and PAE evolution with a 2nd harmonic phase sweep.

efficiency. Different types of topologies are used to design the matching network, such as high-pass, low-pass and bandpass. In our design we are considering the lumped component low-pass topology and performed its designed using the ADS Smith chart utility.

Stability is an important factor in PA design. The stability can be improved at higher frequencies by adding the proper RC to the input matching network [8], usually implying a trade-off between gain and stability.

Input matching is performed from the optimum source impedance obtained from source pulling at 1.75 GHz centre frequency, with the stability network, and the performance is evaluated by variation of the impedance around the band. A Pin diode was included in the input matching network to provide flexibility in tuning. A pre-amplifier [9] with 21.6 dB of gain is used to increase the dynamic range of the PA.

The lumped components for the input/output matching network are chosen with proper Q factor to achieve the highest gain flatness over the band of 1.5 GHz to 2 GHz.

#### F. Simulation Results

A simulation of the design over 1 GHz to 3 GHz at maximum RF input drive of 10 dBm was performed to evaluate the PAE and power delivered to the load. Figure 5 shows that the input reflection coefficient (S11) higher value is -6 dB and the amplifier gain (S21) remains relatively constant at 30 dB over the band of 1.5 GHz to 2 GHz. Figure 6 shows that the PAE performance is always higher than 60% over the band of interest.

These results were then improved upon performing an optimization of the lumped components and of the transmission lines of both input and output matching networks. The results obtained after the optimization are presented as red curves in figures 5 and 7. It can be seen that the reflection coefficient is improved, being the same gain flatness maintained over the same bandwidth. On the other hand, also a better PAE is obtained.

The harmonic distortion of the design was analysed by means of an harmonic balance (HB) simulation at 1.75 GHz with the optimum order of 30 harmonic frequencies. The two highest harmonics (2nd and 3rd) show amplitudes lower than -25 dBm relative to the fundamental. The input referred 1 dB

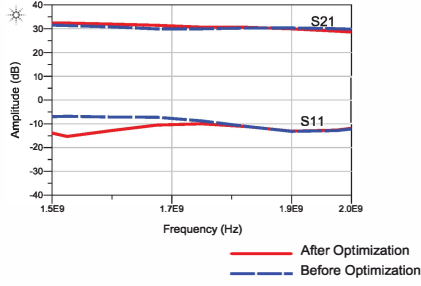


Fig. 5: S-parameters vs frequency.

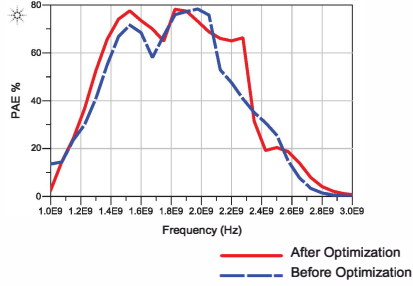


Fig. 6: Curves of the PAE vs frequency characteristic.

compression point is found at 0 dBm. The respective drain current and output voltage waveforms are shown in figure 7. The bifurcation shown in the current waveform is due to the knee voltage effect. This can be rectified by choosing the load-line which prevents the drain voltage from entering into the keen region, with which the DC power consumption remains the same, whereas the RF power is reduced because the output voltage swing is no longer maximized. Thus, the drain efficiency will be sacrificed implying a trade-off between linearity and efficiency.

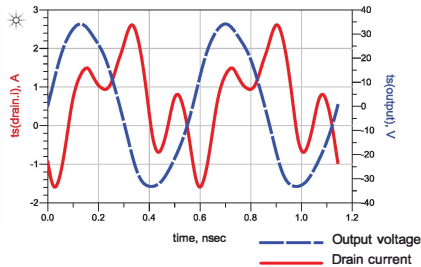


Fig. 7: Drain current and voltage waveforms.

### III. POST LAYOUT RESULTS

The layout of the design, including input and output matching networks, can be seen in figure 8. The substrate being used is a Rogers 4003 with a thickness of 0.5 mm and conductor thickness of  $35 \mu\text{m}$ . The board area is 8.5 cm x 4.5 cm.

After performing an EM simulation on the layout, the respective equivalent layout components could be extracted

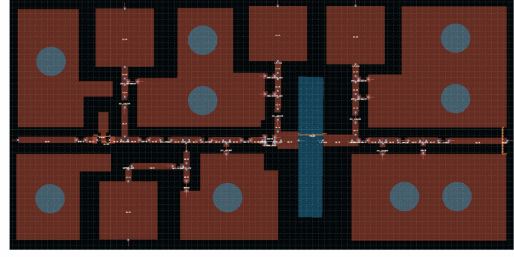


Fig. 8: Layout of the class-J PA, including matching networks.

(figure 9). The performance of the new model including layout components proved to be similar to the optimized results obtained with the schematic version.

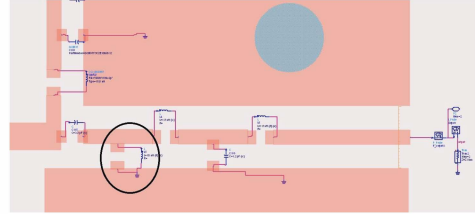


Fig. 9: Schematic including layout components.

A MC simulation was performed on the layout to analyse the variability of the PAE (figure 10) and gain (figure 11) considering a 5% tolerance of the lumped components of the matching networks. It can be observed that the resulting PAE and the S parameters variability is about 10% over the full range of frequencies. This shows that the design is relatively robust to variations of these components.

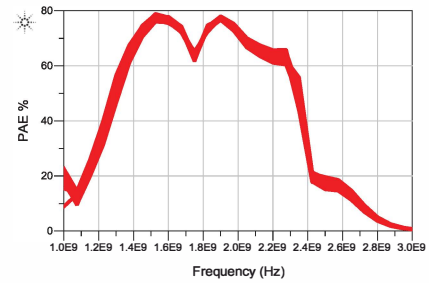


Fig. 10: Monte Carlo simulation of PAE vs. frequency.

On the other hand, PAE is more severely affected by variations of the load impedance, as it can be seen in figure 12 (continuous line) which shows the PAE vs. load variation, at 1.75 GHz frequency and 10 dBm RF input drive. To improve the adaptivity of the design to load variations, a simulation was performed to evaluate how lumped components should be varied in order to maintain high PAE values. From our analysis, it was concluded that the shunt inductor (shown

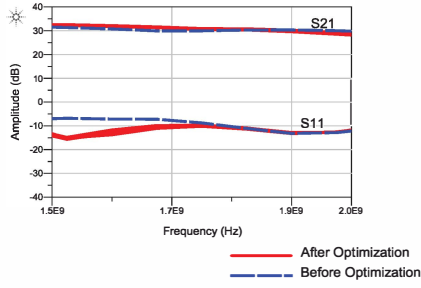


Fig. 11: Monte Carlo simulations of S-parameter vs. frequency.

circled in figure 9) is the element which affects most the performance of the output matching network and, thus, it is the one to be chosen to re-adapt the output matching network for output load variations.

The dashed curve in figure 12 shows the PAE vs. load variation when the shunt inductor is changed from the nominal 2 nH value to 3 nH. It can then be seen that the PAE of the design could be maintained above 70%, even when the load is varied largely from 21  $\Omega$  to 98  $\Omega$ , by shifting the inductor between these two values. This shifting will be performed automatically after detecting a decrease of the output power. This subject is not further explored here.

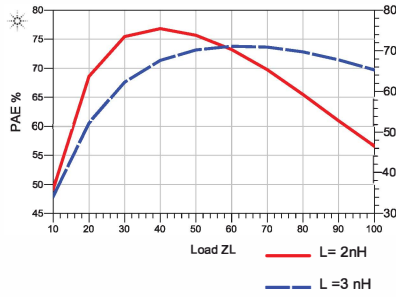


Fig. 12: PAE vs load for different inductor values.

#### IV. EXPERIMENTAL RESULTS

The layout of the Class-J PA shown in the figure 8 was implemented within a Rogers 4003 substrate and mounted on a aluminium (Al) chassis which is used both as a heat-sink and ground plane. The S-parameters measured using a CW signal generated with an Agilent 8703B VNA, at -20 dBm input power in the range 1 GHz to 2.5 GHz, are presented in figure 13. It can be seen that a fairly constant gain is obtained, as foreseen in the simulations, nevertheless lower than the predicted values. It was found that this decrease is due to the pre-amplifier. In the simulations the pre-amplifier was able to provide a gain of 21 dB at +5 V operating voltage, whereas the experimental results show that actually it is unable to provide the gain specified by the manufacturer. Instead of operating at +5 V it operates at a lower 1.9 V, providing a gain of 6 dB already with some distortion at the output. For this reason the

overall gain and output power is 15 dB lower in the measured results.

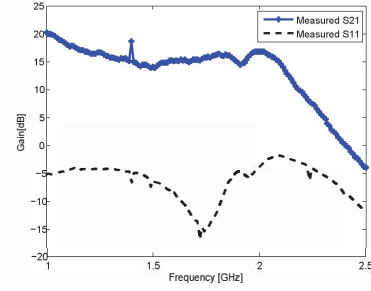


Fig. 13: Measured S21 and S11 parameters with pre-amplifier.

A second prototype was then implemented, now without the pre-amplifier stage, using micro-strip stubs instead of lumped elements in the input and output matching networks. On the picture shown in figure 14 one can see the input and output matching networks, as well as the GaN HEMT connected to the Al heat-sink with screws.

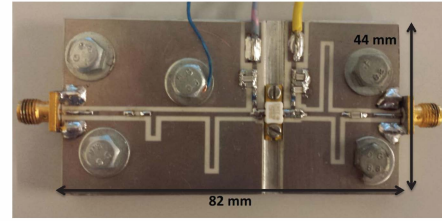


Fig. 14: Prototype of the broadband Class-J PA design.

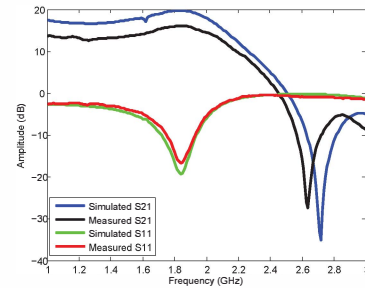


Fig. 15: Comparison of measured and simulated S21 and S11 parameters from the prototype without pre-amplifier stage.

Figure 15 shows a comparison between simulation and experimental results of the gain flatness and return loss, using a CW signal at -20dbm VNA input power in the range 1 GHz to 3 GHz. It can be observed that the experimental gain and output power values are significantly close to the values provided by the simulations, with a 3 dB of gain degradation due to the fabrication process and insertion losses in the cabling used for the measurements.



The maximum PAE is obtained by driving the PA near the compression point that occurs, after the simulations, at 27 dBm input power level. Without the pre-amplifier and due to limitations on the measurement equipment, it was not possible to reach this level. The PAE was evaluated at 1.75 GHz with maximum possible input power of 15 dBm. From figure 16 it can be observed that the maximum PAE obtained is 22% at 15 dBm input power level, which is very close to the simulation results.

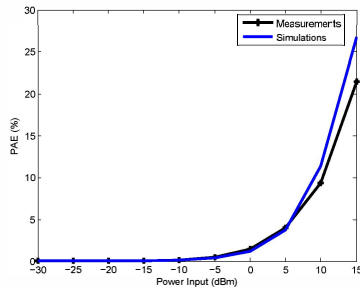


Fig. 16: Evaluation of PAE at 1.75 GHz.

The results obtained with the prototype without pre-amp stage are closely match to the simulation results and it is expectable that with the designed pre-amplifier gain conditions the PA would provide a PAE above 60% over a wide bandwidth at higher input power level, as shown in the figure 10.

## V. CONCLUSION

This paper presents the design of a high bandwidth, dynamic range, efficiency and gain, adaptive class-J power amplifier. The objective is to obtain a PA platform to be used with different communication standards, as well as within applications where the PA load is likely to vary significantly, as it is the case with the use of radio-frequencies in medical treatments. The key feature is to design the PA to operate in a multi-band frequency scenario, maintaining as much as possible the same performance characteristics, including when load impedance changes.

The design steps are presented and results are included which show that a quasi constant gain of 30 dB is ensured in the 1.5 GHz to 2 GHz band, with S11 lower than -10 dBm and PAE always higher than 60%, even when tolerances of the matching network components are considered. In order to ensure that this performance is maintained when impedance load varies, an analysis was carried-out to identify which component(s) should be varied to re-adapt the PA behaviour to the new load conditions. It is shown that switching the value of one component it is possible to maintain the PAE value above 70% even when the load is varied largely from 21  $\Omega$  to 98  $\Omega$ .

These results motivate to explore further dynamic load and source modulation schemes to achieve higher bandwidths in order to meet different application requirements, notably, in the application of cognitive radio and software defined

radio approaches to healthcare applications. Future work to be carried out concerns the characterization of the PA comprising load adaptability using an adaptive output matching network.

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