A Low Power Clocked Integrated-and-Fire Modulator for UWB Applications

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***Abstract*—An integrate-and-fire modulator (IFM) is designed for power scavenging systems like: Wireless Sensor Network (WSN) and Radio Frequency Identification (RFID) sensor tags. The circuit works with a clock in order to be able to be synchronized with microprocessors, which must be used to reconstruct the signal. The modulator is simulated using 130nm CMOS technology and the resulting power consumption is around 14nW at a clock frequency of 10 kHz. The OTA individually dissipates roughly 13nW. Signal reconstruction resulted in a 9.2 ENOB.**

***Index Terms*-- Integrate-and-fire neurons, Low power design, UWB transmission, low power design**

I. INTRODUCTION

Neurons are diverse in terms of functionality and behavior. Among different models, integration-and-fire neuron (IFN) is a simplified version that is reduced to a first order fire-and-reset system [1]. In this view, the aggregated charge from external excitation raises the neuron's cell-membrane potential until it reaches a threshold. Then, the neuron generates a spike and the membrane potential resets to a reference value and again starts accepting inputs from neighboring neurons. Basically, the membrane can be thought as a capacitor that relates the membrane potential (action potential) with the excitation current [1]. The resulting output pulse-density (firing rate) is proportional to the net input excitation. This process, also known as Pulse Density Modulation (PDM), converts the analog input signal to a series of time-encoded spikes, profiting from a dynamic sampling rate [1], [2]. In other words, its function is time encoding that maps the amplitude information, of an arbitrary stimulus, to a series of time distances (δ) between fixed- and short-duration spikes (Fig. 1) [3].

In power scavenging systems like WSN and RFID tags, there is a huge effort to design low-power analog-to-digital converters (ADC) or even sometimes to eliminate it from the transmitter block diagram [4]. Pulse width modulation (PWM) or integrate-and-fire modulation, which is also known as IFN modulator or IFN converter, could be utilized as an ADC replacement [4], [5] and at the same time be regarded as actual encode/modulation scheme. The integrate-and-fire modulation technique can then be used in Impulse Radio Ultra Wide-Band (IR-UWB) transmitters. A study on power efficiency of this transmitter shows that it roughly dissipates 8 times less power than a digital BPSK transmitter [6].

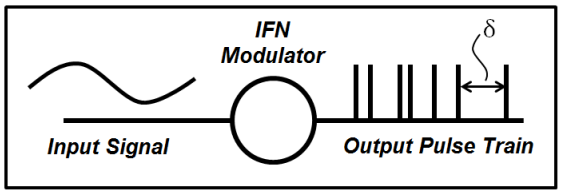

Figure 1. Function of integrate-and-fire neuron as a modulator

In this paper, a low power clocked-based integrate-and-fire modulator has been designed for RFID and WSN systems involving slow varying signals. The rest of this paper is organized as follows: in section II, the circuitry of the modulator will be discussed. In section III, the reconstruction method is completely described. Finally, results have been presented in section IV, followed by a conclusion in section V.

II. CIRCUITRY OF INTEGRATE-AND-FIRE MODULATOR

An integrate-and-fire modulator (IFM) is composed of an integrator, a comparator and a delay circuit as illustrated in Fig. 2. First, the input signal is integrated in time and then compared with a reference voltage (θ), this will be carried out every $1/f_S$ second. As soon as the integration reaches the threshold θ, the comparator activates the switch to reset the integrator. However, this happens after a certain amount of time τ_r, called refractory period generated by a delay circuit, which can be realized by an asymmetric inverter with controllable current on the falling edge. The response for the integrator can be represented as [3]:

$$\int_{t_i+\tau_r}^{t_{i+1}} x(t)dt = \theta\,, \quad \forall i \in \mathbb{Z}\,, \tag{1}$$

where $x(t)$ is the input signal and t_i $(i \in \mathbb{Z})$ is a timing sequence. The minimum sample rate in IFM is related to maximum adjacent interval $(\delta_{max} = sup(t_{i+1} - t_i))$.

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Obviously, the input signal can be perfectly recovered provided that the minimum sample rate is above Nyquist rate, or that is to say $\delta_{max} < 1/f_{Nyquist}$ [3], [7].

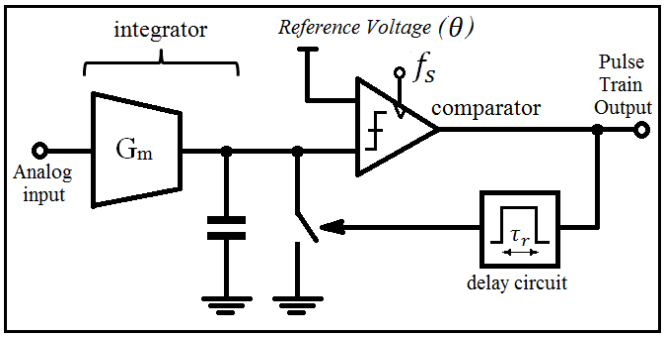

Figure 2. Architecture of the integrate-and-fire modulator

The IFN converter can serve as a baseband modulator in a UWB transmitter. IR-UWB pulses can be used to actually send the IFN spikes. Let us call this communication system Impulse-Radio Integrate-and-Fire (IRIF) transceiver. The IRIF transmitter comprises an IFM and an impulse-radio generator that will send enough number of UWB pulses representing each IFN pulse. The construction of the transmitting signal based on IFN spikes is shown in Fig. 3. Since the pulse generator is deactivated most of the time, power efficiency will greatly improve [6].

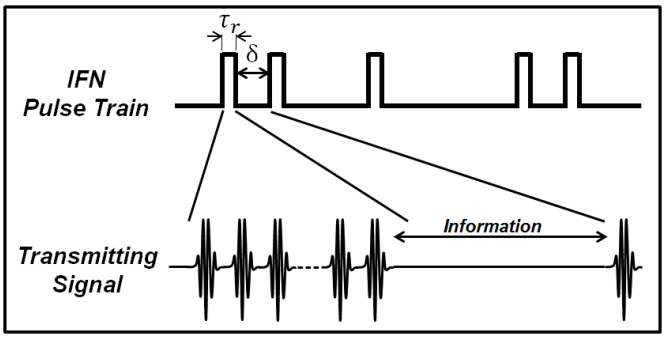

Figure 3. To generate transmitting signal based on output signal of the IFM. A series of UWB pulses represent each IFN pulse.

Sampling rate in conventional ADCs is constant, whereas IFM enjoys a dynamic sampling rate, which depends on the shape of the input signal and it may be either above or at the Nyquist rate [2]. This dynamic sampling rate is inherently non-uniform, leading to significantly better spectrum efficiency. Moreover, by using integrate-and-fire time encoding, lower power consumption is achievable.

A. Gm-C Integrator

An Operational Transconductance Amplifier (OTA) is designed in weak inversion region of operation using a multi-tanh triplet [8]. Multi-tanh topology is chosen to increase the linear input range and its power dissipation is reduced by taking the advantage of designing it in weak inversion. The OTA uses a composite transistor to degenerate the differential pairs, gaining a very small third harmonic distortion (HD3) [8]. The transconductance value is 37nS, with a linear range of 340mVpp, dissipating power of almost 13nW. OTA is the major power consumer circuit block of the whole IFM.

B. Comparator

Latch-type sense amplifiers, or sense amplifier based flip-flops are kind of track-and-latch (T/L) comparators and are widely used in memories, ADCs and on-chip transceivers [9]. They achieve fast decisions due to a strong positive feedback. Since in most practical applications IFN action potentials should be synchronized to a fast clock of a processor, a low power T/L comparator is used in this modulator [10]. It has no static current and therefore suitable for low power circuit. The comparator dissipates roughly 1nW of power at clock frequency of 10 kHz. Its comparison delay is 25 ps and the offset voltage at the input is roughly 10 mV.

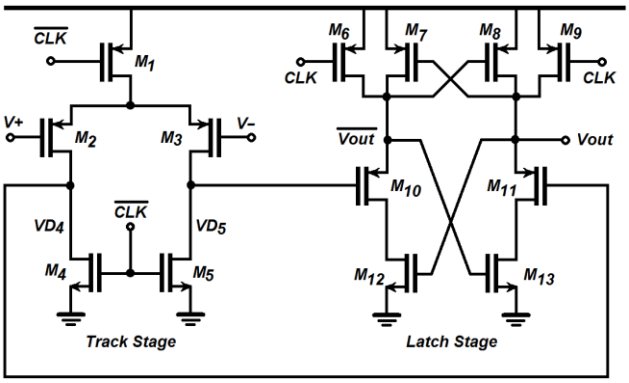

Figure 4. Track-and-Latch comparator

The comparator is composed of two stages, namely track stage and latch stage. The first stage instantaneously tracks the difference between input terminals. The latch stage will store the comparison results. In detail, the comparator functions as follows. First, the clock level is low and because the channels of M4 and M5 are inverted, the nodes VD4 and VD5 are pre-charged "low"; meanwhile V_{out} and $\overline{V_{out}}$ are pre-charged "high", and M6 and M9 are on. In a rising clock edge current flows through M1 and charge the intrinsic capacitors in nodes VD4 and VD5. Depending on input voltages and their difference, one of the capacitors will charge faster than the other, turning on either M10 or M11. As long as the clock is high the data is latched at the output.

C. Delay Circuit

The delay circuit is responsible for providing enough refractory time letting the capacitor discharge completely. The circuit can be easily realized as shown in Fig. 5. It is basically an inverter with a delay in the falling edge, which is generated through current starvation controlled by a MOSFET. By using the current controller, the falling edge becomes smoother and, therefore, the last two inverters seen in Fig.5 are utilized to provide correct logic and create a sharp transition at the output.

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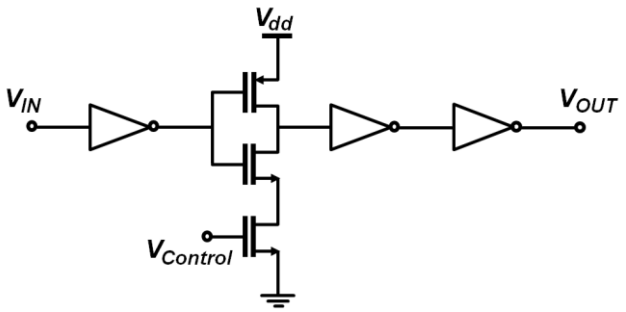

Figure 5. Delay circuit: a current controller inverter

III. Signal Reconstruction Method

Several approaches can be adopted to reconstruct the original signal based on the received spikes, either in time-domain [7], [11] or frequency-domain [12]. However, a simple recovery algorithm is used [7] to verify the performance of the modulator, which has been carried out by MATLAB. Since any band-limited signal can be expressed as a low-pass filtered version of an appropriately weighted sum of delayed impulse functions [10], [13], for an Ω_s-bandlimited signal x(t), which has k ($k \in \mathbb{Z}$) IFN spikes within length of l ($l \in \mathbb{Z}$), equation (2) can be used to decompose the signal into spike trains.

$$x(t) = h(t) * \sum_{j=1}^{k} \omega_j \delta(t - s_j) = \sum_{j=1}^{k} \omega_j h(t - s_j) \quad (2)$$

In equation (2), $s_j = (t_{j+1} + t_j)/2$, $\omega_j = x(s_j)$ and $h(t)$ is the impulse response of the ideal low-pass filter represented in equation (3) and ′*′ represents the convolution operator.

$$h(t) = \frac{sin\Omega_s t}{\pi t} \quad (3)$$

Denoting by $[q]_l = x(t_l)$ and the vector of weights $[W]_k = [\omega_j]$, equation (2) can be rewritten in a matrix form as follows:

$$\boldsymbol{q} = \boldsymbol{H^T W} \quad (3)$$

where T denotes the transpose and $[H]_{k,l} = [h(t - s_j)]$ is a matrix where each row gives the vector of an s_j-shifted impulse response of the ideal low-pass filter with bandwidth slightly bigger than Ω_s. If the weights are known, the signal can be recovered. Substituting equation (2) into equation (1), we obtain:

$$\theta_i = \sum_j \omega_j \int_{t_i}^{t_{i+1}} h(t - s_j) dt = \sum_j \omega_j c_{i,j} \quad (5)$$

where $c_{i,j}$ are coefficients of a matrix where its columns give the values of integrals for each s_j-shifted $sinc$ over all $[t_i, t_{i+1}]$ and can be numerically calculated from the following equation.

$$c_{i,j} = \int_{t_i}^{t_{i+1}} h(t - s_j) dt \quad (6)$$

So, the weights are simply computed by $\boldsymbol{W = C^{-1}\theta}$ and finally using equation (4), the input signal can be reconstructed as follows:

$$\boldsymbol{q = H^T C^{-1}\theta} \quad (7)$$

IV. Simulation Results and Discussion

The proposed clocked based IFM is designed in the 0.13um technology node with 1.2V power supply (technology voltage). The total average power consumed by the modulator is around 14nW at 10kHz clock frequency, and shows a linear dependency on frequency. In some recent publications, the power dissipation has not been considered as a major concern [7]; however, CMOS-based IFN modulators with 100uW and 300nW power consumptions are respectively reported in [11] and [15].

Figure 6 illustrates how the signal is recovered using a clock frequency of 100 kHz applied to the comparator, while the reference voltage is set to 100mv. In order to test the circuit, a sine wave with frequency of 20Hz has been applied to the circuit, which can be seen in Fig. 6-a. Time encoded pulse train generated by IFM is illustrated in Fig. 6-b. With 100mv reference voltage, around 25-to-30 IFN spikes will be created in each period of the input sine wave. Figure 6-c shows the reconstructed signal. The Signal to Error power Ratio (SER) is 57dB and ENOB of 9.2 has been achieved. The error is demonstrated in Fig. 6-d, which is the difference between input signal and the reconstructed one. As the clock frequency increases, the time resolution between spikes will increase so that the reconstruction quality will improve and higher ENOB is achievable.

Quality of the signal reconstruction and more details are given in TABLE I for the case of Vref=100mv. The quality of the reconstruction of the signal also depends on the harmonic distortion of the OTA and the precision of the reconstruction algorithm. In order to obtain an ENOB of 9.2 almost 28 IFN spikes are required. However, a digital BPSK transmitter needs to send 368 bits to reach the same ENOB as IR-IF transmitter. Therefore, the proposed communication system

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consumes less power comparing to an ordinary BPSK transmitter.

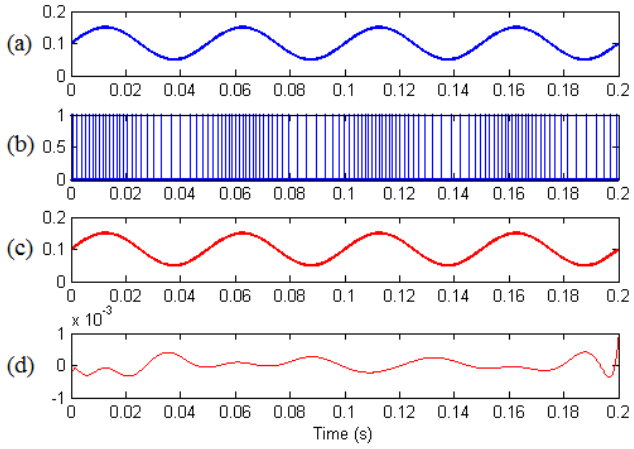

Figure 6. Signal reconstruction. (a) Input signal: a 20Hz sine wave. (b) Integrate-and-Fire pulse trains generated based on input signal using IFM. (c) Reconstructed signal. (d) Error between the original and reconstructed signal.

TABLE I. TABLE TYPE STYLES

Clock Frequency	ENOB	SER	Spike per period
10 KHz	5.1	32dB	26
100 KHz	9.2	57dB	28

V. CONCLUSION

A clocked-based monophasic IFM has been designed in 0.13um technology. This modulator can be used in WSN, RFID sensor tag applications and generally in those systems dealing with slow varying signals. The results show that the power consumption of the whole modulator is as low as 14nW at 1.2 V. Using MATLAB signal has been recovered perfectly with power ratio of SER =57dB and ENOB of 9.2.

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