A Low-Power Analog Adder and Driver Using a-IGZO TFTs

Pydi Ganga Bahubalindruni, Vítor Grade Tavares, Rodrigo Martins, Elvira Fortunato, and Pedro Barquinha

***Abstract*— This paper presents a novel low-power analog circuit, with n-type IGZO TFTs that can function as an adder operator or be designed to operate as a driver. Experiments were set to show summation of up to four signals. However, the design can easily be expanded to add higher number of signals, by appending a single TFT at the input per each additional signal. The circuit is simple, uses a single power supply irrespective to the number of input voltage signals, and shows good accuracy over a reasonable range of input values. By choosing proper TFT dimensions, the topology can replace the typical output drivers of TFT amplifiers, namely the common-drain with current source biasing, or the common-source with diode connected load. The circuit was fabricated with a temperature that does not exceeds 200 °C. Its performance is characterized from measurements at room temperature and normal ambient, with a power supply voltage of 12 V and a load of ≈ 4 pF. The proposed circuit has shown a linearity error less than 3.2% (up to an input signal peak-to-peak value of 2 V), a power consumption of 78 µW and a bandwidth of ≈ 115 kHz, under worst case condition (when it is adding four signals with the same frequency). It has shown superior performance in terms of linearity when compared to the typical drivers considered in this study. In addition, it has shown almost the same behavior when measurements were repeated after one year. Therefore, the proposed circuit is a robust viable alternative to conventional approaches, being more compact, and contributes to increase the functionality of large-area flexible electronics.**

***Index Terms*— Analog adder, driving circuits and linearization, IGZO TFTs.**

I. Introduction

INDIUM-Gallium-Zinc-Oxide thin-film transistors (IGZO TFTs) exhibit an assortment of characteristics that make them very attractive for the next generation of large scale electronics. Compared to other competing technologies, namely, a-Si:H and OTFT (organic-TFT), IGZO devices present good optical transparency and a relative higher mobility. Besides the natural field of application– display technology– its cost effectiveness and the possibility to deposit circuits on unconventional substrates (such as plastic) motivates its use in different applications and in various fields [1]–[3]. Given that devices can be fabricated at low temperature, they are also excellent candidates for the next generation of flexible electronics [4]. This realm of distinctive possibilities is stimulating the research of analog mixed-signal circuits with thin-film technologies [5]–[7].

Thin-film technologies based on low temperature fabrication processes are key enablers of new promising solutions, as described, but not without its own shortcomings. The lack of stable complementary devices (p-type) [8], [9] and orders of magnitude lower field-effect mobilities, compared to crystalline semiconductor technologies, makes the design of analog circuits a challenging task. It limits the scope to relatively low frequency operation, and attaining high gain is difficult, which is frequently fulfilled through less customary techniques, such as the use of positive feedback or bootstrapping for g_m cancellation [5], [10]. Nevertheless, there are a variety of needs for low-frequency signal processing circuits, especially at sensor front-ends. Many sensors either follow the same fabrication processes and/or use the same materials as TFTs. Having electronics and sensors built on a single process is highly cost effective, which fully justifies the investment in the development of analog circuits.

The realization of analog adder operators is of considerable interest for signal processing in linear analog circuits [11], neural networks [12], continuous time signal processing applications [13] and oversampling data converters [14]. Although significant work has been described in literature with CMOS technologies [15]–[17], reports on adders using IGZO TFTs are scarce. The work proposed in [5] is an example of a simple circuit based on TFTs for this purpose. However, it is limited to the summation of just two signals. In its present form the circuit imposes limitations on the external stimulus, because one of the inputs needs to be set as an exact multiple value of another. In addition, accurate phase has to be maintained between the stimulus and its corresponding multiple. If the number of input signals are to be increased, the limitations on stimulus become even more stringent.

This paper presents a novel linear analog adder devised solely with n-type IGZO TFTs. The proposed circuit provides a simple way of adding 'n' number of signals and produces a single output without resorting to an operational amplifier. A source degeneration technique is used to improve the linearity performance of the circuit. In addition, care has been taken to compensate the gain loss from this linearization method by using a simple output subtracter stage.

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The implementation of driver circuits with TFTs is still not well addressed in literature. However, the proposed circuit can also be used as an output driver with improved linearity when compared to the common-drain (CD), and common-source (CS) with a diode connected load, which are the typical output topologies utilized in TFT circuits.

The remaining of the paper is organized as follows: Section II presents the device fabrication details. Section III describes the circuit design and Section IV explains the details of circuit stability analysis. Sections V and VI illustrate the proposed circuit as a driver and present the respective measured results and discussion. Finally, conclusions are drawn in Section VII.

II. Device Fabrication and Characterization

TFTs employed in this work have a bottom-gate inverted staggered structure, being fabricated on corning eagle glass substrates. The gate electrode was e-beam evaporated and patterned by lift-off, consisting of 60 nm thick Ti/Au. A 250 nm thick dielectric following a multilayer approach consisting of SiO_2+ Ta_2O_5+ SiO_2 was then RF sputtered and patterned using reactive ion etching. This was followed by the deposition and lift-off patterning of RF sputtered IGZO layer, 40 nm thick. Source/drain electrodes were processed with Ti/Au following a similar procedure of that described for the gate electrode. Finally, devices/circuits were passivated with spin-coated SU8 transparent resist. Annealing in air at 200 °C for one hour was carried out prior passivation. All TFTs in the circuit have a channel length of 20 µm and a gate to source/drain overlap of 5 µm. These devices have shown a mobility of 17.4 $cm^2V^{-1}s^{-1}$, gate leakage current in the order of pA [18], and a turn-on voltage of −1.5 V. Transfer and output characteristics of a TFT with width = 80 µm and length = 20 µm are presented in Fig. 1.

It has to be noted that the transparent devices and circuits can be achieved by employing transparent conductive oxides (e.g. IZO, ITO) as gate, source, drain electrodes and interconnects. However, this work used Ti/Au for source/drain as it facilitates wire-bonding for easier and flexible testing.

III. Circuit Design

The proposed circuit schematic and its micrograph before and after wire-bonding are presented in Fig. 2. This circuit is capable of adding several inputs. However, the fabricated circuit was designed to add up to four voltage signals. As it can be noticed from Fig. 2(a), in order to enhance the ability of the circuit to add more number of voltage signals, a single TFT should be added to the input block (parallel to T1, T2 or Tn) for each additional input, without any other structural changes.

In terms of circuit operation, the diode connected TFT (TB1) acts as a source degeneration resistor with an equivalent impedance of $1/g_{mB}$, where g_{mB} represents the transconductance of TB1. This TFT helps improving the linearity performance of the circuit due to negative voltage feedback. However, this imposes a limitation on the gain of the circuit, which is compensated by the output stage formed by TO1 and TO2. A closer look into the first stage reveals that

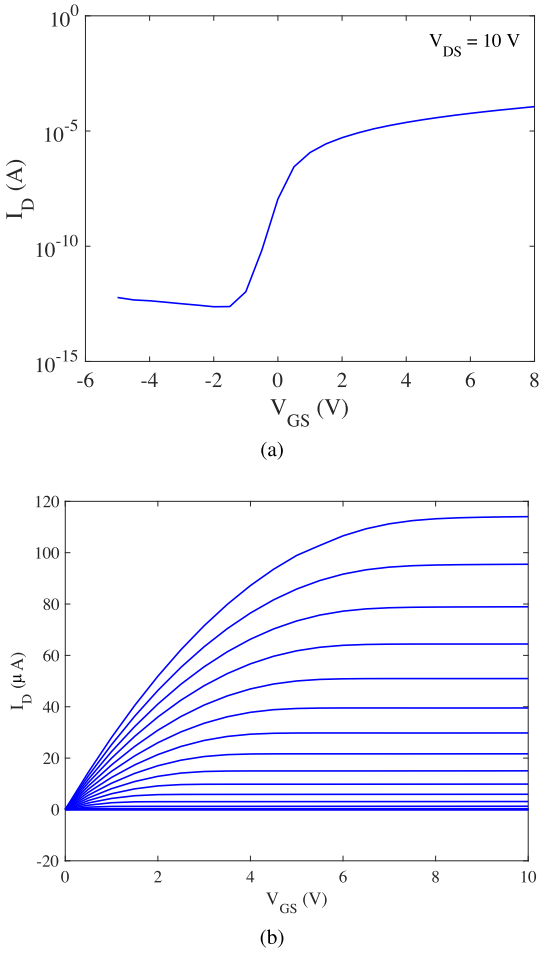


Fig. 1. Measured IV characteristics of a TFT with width = 80 µm and length = 20 µm (a) Transfer characteristics under saturation. (b) Output characteristics when V_{GS} is swept between 0 to 8 V.

it acts as a phase splitter, its output signals v_{o1} and v_{o2} are in phase opposition. Subsequently, the output stage carries out a subtraction of these two signals performing a differential to single ended conversion. The subtraction operation that produces v_o consequently attenuates the even harmonics that might be present in v_{o1} and v_{o2}, which further improves the overall linearity of the circuit.

The small-signal equivalent circuit, formed by transistors T1 to Tn, TB1 and TB2, is shown in Fig. 3. Since transistors are designed with a relatively large channel length, channel length modulation is ignored in the analysis. Assuming the same aspect ratios for all transistors, T1 to Tn, and under similar bias conditions, they will share the same small-signal transconductance value g_m, while the load and source degeneration transistors will be defined by g_{mB}. With the help of Fig. 3, the relationship between the output and input voltages can be derived as follows,

$$\begin{aligned} v_{o1} &= -v_{o2} \\ v_{o2} &= \frac{1}{g_{mB}}[g_m(v_1 - v_{o2}) + g_m(v_2 - v_{o2}) \\ &\quad + \cdots + g_m(v_n - v_{o2})] \\ v_o &= v_{o1} - v_{o2}, \quad \text{hence} \\ v_o &\propto -(v_1 + v_2 + \cdots + v_n) \end{aligned} \tag{1}$$

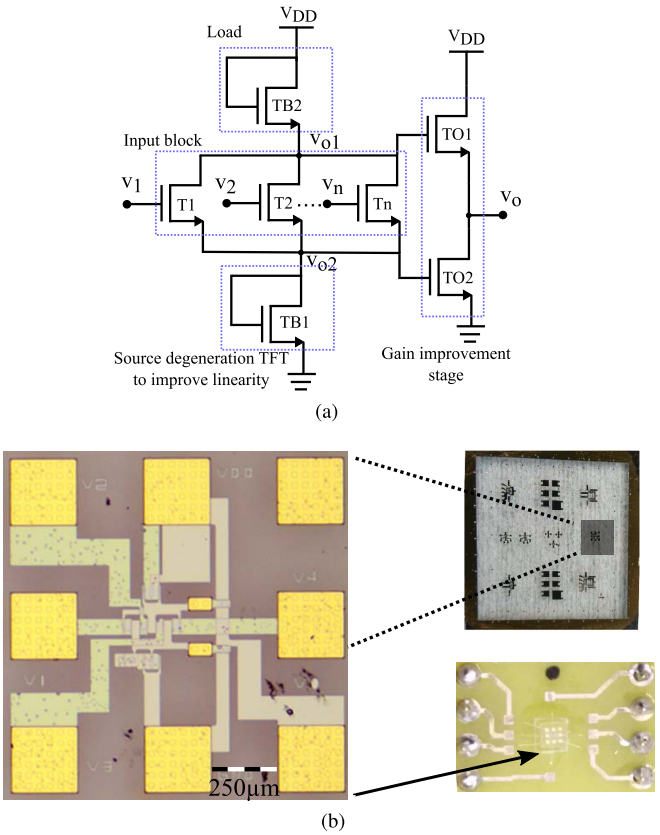


Fig. 2. Novel adder: (a) Circuit schematic. (b) Micrograph of the fabricated circuit and a glass substrate containing many analog circuits and a photo of wire bounded circuit.

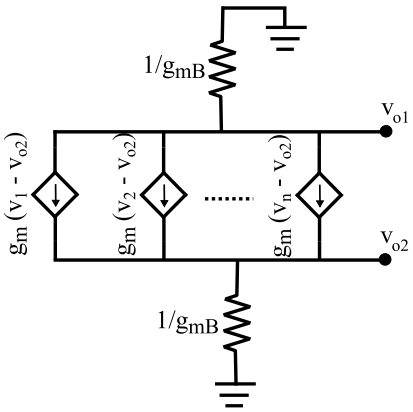


Fig. 3. Small signal equivalent of the circuit (excluding the output stage).

For the specific case when $g_{mB} = ng_m$, i.e., $W_{(TB1/TB2)} = nW_{(T1,T2..Tn)}$, equation (1) can be reduced to

$$v_o = \frac{1}{n}\left[v_1 + v_2 + \cdots + v_n\right] \tag{2}$$

From (1), it can be concluded that this circuit can perform the summation of multiple signals. The average of the input signals can also be obtained as per (2). Nevertheless, one should realize that whenever expanding the number of inputs, the bias current increases. All transistors should be kept in saturation, by proper biasing, and so they can always be re-sized to compensate that effect. For the same reason, expandability also imposes limitation on signal amplitudes. Eventually the maximum number of signals will be defined by the type of signals, power supply and TFT parameters.

IV. Circuit Stability Analysis

Oxide TFTs are relatively stable compared to a-Si:H [19]. However, shifts in the threshold voltage (ΔV_{TH}) of oxide TFTs can be a result of either bias stress [20], [21] or aging [22]. Charge trapping close to the dielectric and semiconductor interface can result in ΔV_{TH} due to bias stress. On the other hand, generation of donor-like states increases the conductivity of the channel and can lead to ΔV_{TH} due to aging [22]. The gate bias stress impact on V_{TH} of devices that are fabricated in our lab (where the present circuits fabrication also took place), is reported in [20], [21]. Though the gate bias stress impact on ΔV_{TH} is reversible by resting the devices for several hours [21], it is important to include ΔV_{TH} cancellation techniques in the analog/mixed-signal design, in order to guarantee a stable long-term circuit operation.

For the sake of simplicity, threshold voltage variation with respect to time (stress time or aging) is expressed as follows:

$$V_{\mathrm{TH}}(t) = V_{THi} + \Delta V_{TH}(t) \tag{3}$$

Considering the output stage, which is formed by TFTs TO1 and TO2, from a large signal analysis perspective and assuming that the TFTs have same dimensions and are well matched, one can obtain:

$$k\left[V_{o1} - V_o - (V_{THi} + \Delta V_{TH}(t))_{TO1}\right]^2 = k\left[V_{o2} - (V_{THi} + \Delta V_{TH}(t))_{TO2}\right]^2 \tag{4}$$

which results in,

$$V_o = V_{o1} - V_{o2} - \left[(\Delta V_{TH}(t))_{TO2} - \Delta V_{TH}(t))_{TO1})\right]$$

If TO1 and TO2 are exposed to the same conditions, the output signal is almost independent of the $\Delta V_{TH}(t)_{TO1/TO2}$. Similar analysis can be applied to the first stage that is formed by T1, TB1 and TB2. When these TFTs are well matched and having the same dimensions, V_{o1} and V_{o2} are almost independent of $\Delta V_{TH}(t)_{T1/TB1/TB2}$. Accordingly, the circuit is expected to be robust against the bias stress and aging effects.

V. Circuit as a Driver

By making TFTs at the output stage wider compared to the remaining, and choosing different dimensions for the bias TFTs (TB1 and TB2), the proposed circuit can even operate as a driver with good linearity. Fig. 4 shows a simplified circuit schematic of the driver. It basically corresponds to that of Fig. 3 with just a single input transistor. Taking Fig. 5 as reference, the driver should be able to drive more current to the output, with a given load, through TO2 whenever the output drops below the reference, while TO1 should have its current proportionally decreasing. The opposite should occur when the output rises above the reference. This behavior approaches the typical "push-pull" response, which favors efficiency.

In fact, if properly designed, such behavior can be induced. Observing closely Fig. 5(a), V_{o2} will follow the input in

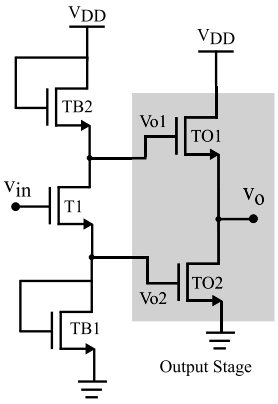


Fig. 4. Simplified schematic of the proposed circuit for driver operation.

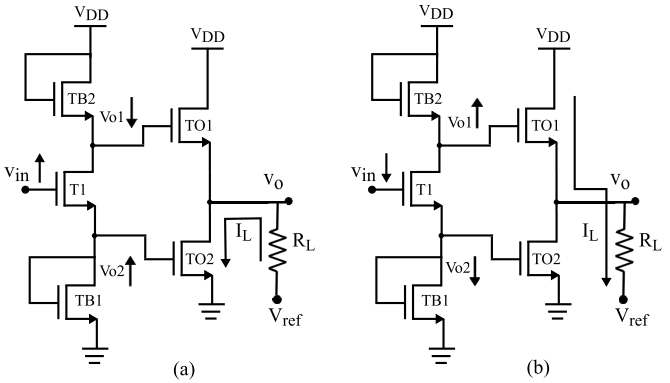


Fig. 5. Proposed circuit operation as a driver for (a) Positive input voltage; (b) negative input voltage.

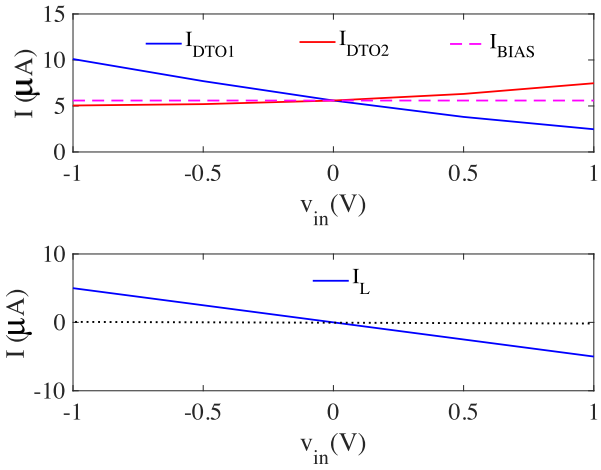


Fig. 6. Current in the TFTs from output stage and the load.

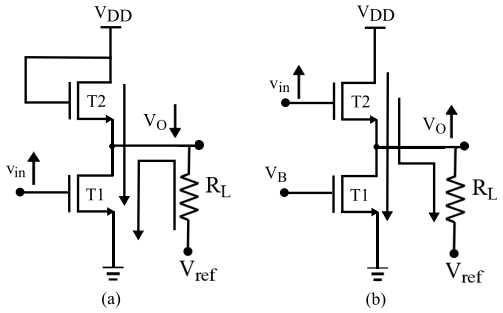


Fig. 7. Current flow direction (a) CS amplifier (b) (a) CD amplifier.

phase, while V_{o1} will be in phase opposition (due to the phase splitting effect of T1). Accordingly, if V_{in} rises above the DC bias, the current flow through the cascade of input transistors, TB1, T1 and TB2, will increase. Then, through the current mirroring effect, TO2 will be driving more current and conversely TO1 will conduct less current. The net balance is a load current flowing from the reference, and the output voltage drops below it. For the present phase of operation, the rate at which the current decreases in TO1 can be controlled with the relative sizes of TB2 and TO1; by designing the first transistor wider a faster drop on V_{GSO1} will be imposed, and consequently its current. When V_{in} increases, the same reasoning applies, but now in the opposite direction — TO1 will drive more current while TB2 less. When the circuit is simulated with the oxide TFT models, the expected response was noticed as it can be observed from Fig. 6.

A. Reference Driver Circuits

To better understand the benefits that the new circuit brings, in relation to more established methods of assembling amplifier output stages with TFTs, two common driver circuits were also fabricated: the CS with diode connected transistor as load and a CD configuration with current source biasing. Both are plotted in Fig. 7. The purpose is to directly confront the linearity of all three configurations. It should be noted that the "push-pull" effect is not evident in these topologies, making them less efficient. In fact, for the CS, when the load current is negative (coming from the load into the driver), the current will even increase in the diode connected transistor as the absolute resistor load-current increases. In the CD, the driver transistor will have to handle both the bias current (always constant) and the positive load current. The circuits were designed to handle similar loads.

VI. Results and Discussion

A. Circuit Setup for Testing

As noted in Fig. 2, several analog circuits and other individual components were fabricated on a shared 2.5 × 2.5 cm^2 corning glass substrate. To facilitate flexibility in testing, the chip was diced into individual circuits and each of them was carefully protected from glass particles that scatter during the cutting process. Finally, all tested circuits were subjected to wire-bonding. More details on circuit preparation for testing and wire-bonding can be found in [10]. Thereupon, all circuits were characterized in normal ambient conditions and at room temperature. Simulations were carried out with an in-house model [23], and circuit measurements were taken with a power supply of 12 V and a load of approximately 4 pF (this load comes from the input of an external unity gain buffer, whose frequency response is much higher than the measured range). Single channel arbitrary function generators (AFG3021B) and

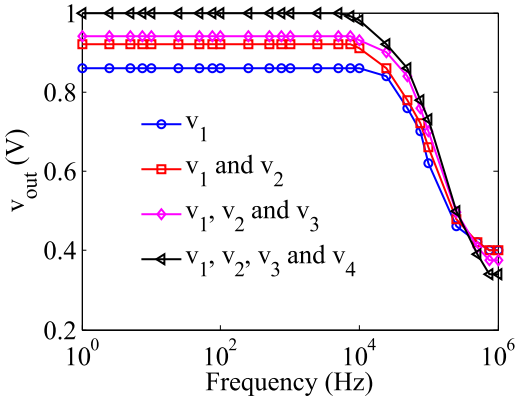


Fig. 8. Measured frequency response of the circuit with different number of input signals (n = 1, 2, 3 and 4), each with a magnitude of A = 1 V.

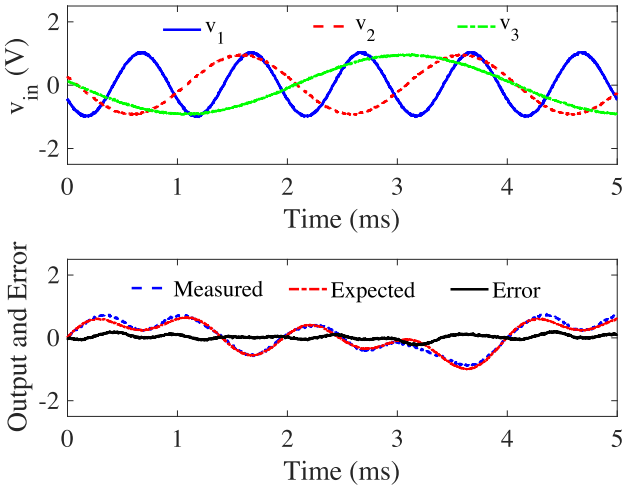


Fig. 9. Circuit characterization from measured and expected response in normalized form.

four channel digital storage oscilloscope (DS2024B) were used for the measurements. The adder circuit is tested with the following stimulus (A = 1 V):

$$\begin{aligned} v_1 &= 5 + A \cdot sin(2\pi f_1 t), \\ v_2 &= 5 + A \cdot sin(2\pi f_2 t), \\ v_3 &= 5 + A \cdot sin(2\pi f_3 t), \\ v_4 &= 5 + A \cdot sin(2\pi f_4 t). \end{aligned} \tag{5}$$

The excitations were set to values that drive the circuit into a region of operation that can be considered linear (relative error $< 3.2\%$).

B. Measurement results

Fig. 8 presents the adder frequency response when different number of inputs are applied. The circuit has shown approximately 115 kHz bandwidth and 78 µW power consumption, when all input signals are active.

The normalized measured response is compared and validated with the expected response in Fig. 9, when

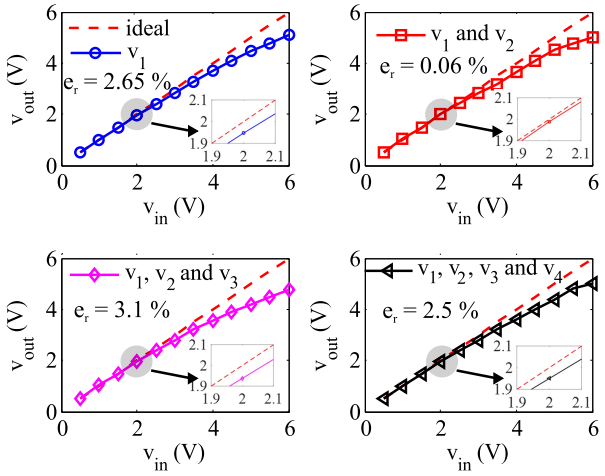


Fig. 10. Measured linearity response of the circuit with different number of input signals. Inset shows the zoomed part at v_{in} = 2 V, where the relative error e_r is calculated.

TABLE I
DIFFERENCE BETWEEN FIRST AND SECOND HARMONIC LEVELS IN (dB)

No. of signals	Proposed circuit	CS amplifier	CD amplifier
1	42	15.2	30
2	36	-	-
3	35	-	-
4	32	-	-

f_1 = 250 Hz, f_2 = 500 Hz, f_3 = 1000 Hz and v_4 is a constant bias.

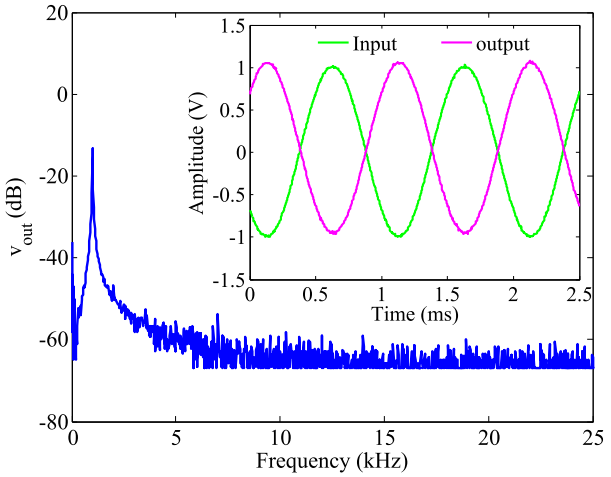
The ideal and measured DC characteristic of the proposed circuit is also presented in Fig. 10, when different number of input signals are applied. The circuit shows a relative linearity error of $e_r < 3.2\%$, until the input signal peak-to-peak value is 2 V, as shown in Fig. 10. The linearity error is defined as e_r = (Ideal value − Obtained value)/(Ideal value).

The CS and CD amplifier circuits (Fig. 7) were also characterized under the same testing conditions as the proposed circuit in order to provide a fair comparison. For all three circuits, the measured output signal (in inset) and its corresponding FFT are presented in Fig. 11 for an input signal amplitude of 2 V peak-to-peak, and a frequency of 1 kHz. It should be noted that the measured response of the proposed circuit is obtained when all four inputs are applied.

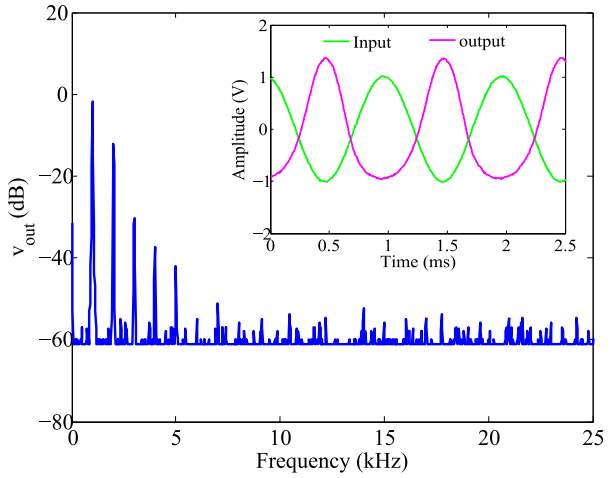
Table I presents the difference between the fundamental and second harmonic components, when different number of input signals (amplitude 2 V peak-to-peak) are applied to the proposed circuit. Similar results can also be observed for the CS and CD amplifiers with the same input signal.

C. Discussion

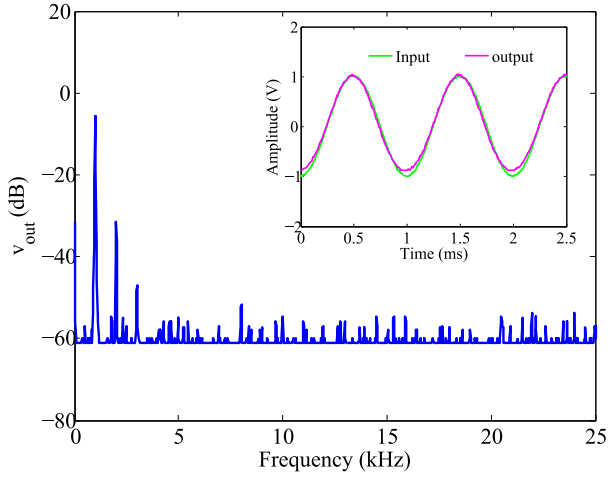
The frequency response of the circuit (see Fig. 8) shows non-uniform intervals in magnitude with different number of input signals. This is because, when some signals are active, the other input transistors were simply cutoff. It means that at anytime a new signal is added (for example, when passing from a setup of $v_1 + v_2$ to $v_1 + v_2 + v_3$) a new transistor is activated and properly biased (in this example, T3).



(a)



(b)



(c)

Fig. 11. Measured circuit response under same testing conditions, when the input signal peak-to-peak value is 2 V and frequency is 1 kHz. (a) Proposed circuit with four inputs enabled; (b) CS amplifier with diode connected load; (c) CD amplifier.

Consequently, the overall circuit bias conditions change with respect to the number of inputs. Under these circumstances, bias current increases and affects the small signal parameters

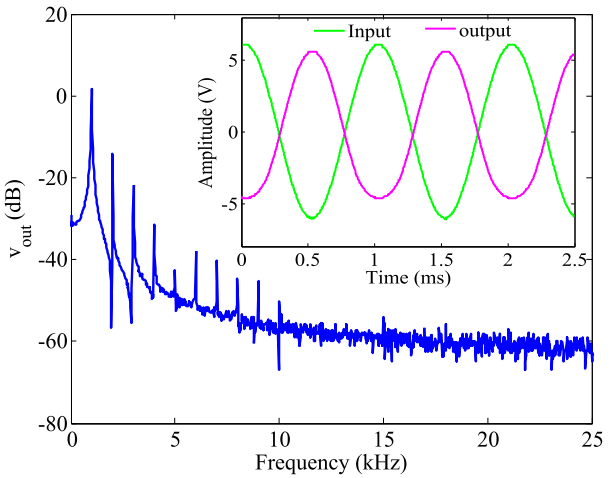


Fig. 12. Measured circuit response, when all the input signals peak-to-peak value is 6 V and frequency is 1 kHz.

of all TFTs, thus also the gain. This testing procedure is followed to avoid the influence that other input transistors, those without input signal in a given experiment, would have in the AC performance. Nevertheless, the normalized summation result shows proper functionality, as can be noticed from Fig. 9. However, it should be noted that if all transistors in the input block were initially biased in the same condition, the circuit would show uniform intervals in magnitude. The bandwidth of the proposed circuit decreases with the increase in number of inputs as expected, due to extra transistor parasitics. The circuit has shown a typical bandwidth range of any other oxide TFT based circuits ($\approx$ 115 kHz).

Similarly, from Fig. 10, it can be noticed that e_r is higher in the case of three inputs when compared to the case of four input signals. This is mainly caused by mismatches (either TFT dimensions or threshold voltages) between devices due to unavoidable process variations. This also shows some impact on the non-uniform intervals observed in Fig. 8.

Considering the proposed circuit as a driver, with a single input signal, the linearity performance can now be compared with both CS and CD amplifiers. For this purpose, take Fig. 11 as reference, where the harmonic representation of the response of each circuit to a sinusoid is presented. In case of the proposed circuit, the difference between the fundamental and second harmonic components is 42 dB. On the other hand, the CS amplifier shows the highest non-linearity (15.2 dB) among all, while the CD amplifier shows a moderate non-linearity (30 dB). These results clearly demonstrate that the proposed circuit linearity performance is superior compared to the others.

In order to test the performance limits of the proposed circuit, all the input signals amplitudes are increased to a peak-to-peak value of 6 V. As it can be observed in Fig. 12, the circuit response is becoming distorted because of the non-linear behavior of TFTs. In this case the second harmonic is just 18 dB below the fundamental component. However, at this voltage level, the CS and CD amplifiers would present much worse performance.

As the analysis in Section IV anticipated, the circuit has shown almost the same performance metrics (within 5% variation) when the measurements are repeated after one year, reinforcing the robustness of the design.

VII. Conclusions

For the first time a novel and low-power analog adder circuit with only n-type IGZO TFTs is designed and characterized from measurements. This design does not need any operational amplifier. Further, the circuit has shown the ability to add up to four signals, however it can be easily extended to more number of input signals without any major changes. This circuit can also operate as a driver, as long as proper dimensions of TFTs are considered. It has shown superior linearity performance compared to the reference driver circuits, because of two reasons: (1) phase splitting and subsequent subtraction operation in the output stage, (2) negative feedback due to simple source degeneration approach (using a diode connected transistor). Reference driver circuits (CS and CD amplifiers) were also fabricated and tested under same conditions for comparison purposes. In addition, the proposed circuit has shown robust performance against aging. From measurements, it was noticed that the linearity error is less than 3.2% for input signals with a peak-to-peak voltage values of 2 V, when adding the total four signals. Under the same testing condition, the circuit has shown a power consumption of 78 μW and a bandwidth of $\approx$ 115 kHz. Based on these performance metrics it can be understood that the circuit could find potential application in next generation flexible low-cost wearable technology to process biological signals.

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