# A comparative analysis and implementation of various PLL techniques applied to single-phase grids

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***Abstract*--The scope of this work is to find the best approach to control advanced inverters used to connect electric vehicles to the grid. Phase-locked Loop (PLL) is a grid voltage phase detection that makes use of an orthogonal voltage to lock the grid phase. This method is suitable for both single and three phase systems, although in single-phase, because they have less information, more advanced systems are required. The easiest way to obtain the orthogonal voltage system is using a transport delay block to introduce a phase shift of 90 degrees with respect to the fundamental frequency of the grid voltage. This method is known as Synchronous Reference Frame PLL (SRF-PLL). The use of inverse Park transformation is also possible. To lower the complexity and increasing the filtering of the output signals, methods using adaptive filters are a good alternative. For this approach, the use of a second order generalized integrator (SOGI) or Adaptive Notch filter combined with PLL, Enhanced PLL (EPLL) and Quadrature PLL (QPLL), leads to satisfactory results.**

***Index Terms*ð Phase Locked Loop, Phase Estimation, Tracking Loops, Negative feedback, Smart grids, Electric vehicles, Grid Synchronization, Grid distortion.**

## I. Introduction

THE number of non linear charges connected to the electric grid is experiencing a fast growing. This phenomenon leads to the development of more demanding equipment to interact with the grid in order to reduce distortion and to meet the operation boundaries defined by standards. Electric Vehicles will represent a great percentage of these kinds of charges, [1], together with the connection mode V2G. Researching for more advanced methods to interact with the grid is of key interest.

This work is supported by Fundo de Apoio à Inovação (Ministério da economia, da inovação e do desenvolvimento), within the framework of the project REIVE ï Redes Eléctricas Inteligentes com Veículos Eléctricos (Smart Grids with Electric Vehicles).

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Numerous methods for synchronization and tracking of the fundamental elements of the grid have been presented in the specialized literature, [2-6]. Those synchronization methods should have a set of characteristics in order to be compliant with the standards and give performance to the converter chain. In this work the searched characteristic are:

- Robustness with respect to noise, stationary and transient disturbances;
- Capability to follow amplitude grid voltage-variations in case of voltage sags;
- Accurate performance in case of grid-frequency variations;
- High filtering performance in case of harmonics distortion;
- Easy analog/digital and hardware/software implementations.

Having this in mind, all the analysis and experiments are conducted to give a choosing pattern for the four main PLL methods used. The Figures and tables presented allow for a fast and accurate decision.

This paper presents a comparative study of the main PLL algorithms for its application to grid-connected power converters. The contributions of this paper can be summarized as follows: Extensive analysis and discussion regarding the key factors to choose an appropriate PLL method to interact with advanced power converters connected to single-phase grids. Section II presents an overview of the PLL algorithms and the analysis of computational requirements. Some considerations regarding the tuning of PLL loops are developed at section III. Section IV provides simulations results that allow concluding about the performance of each method under distorted and non-distorted grids. A summary of results and concluding statements are provided in section V.

## II. PLL Techniques based on In-Quadrature Signals

A block diagram of the basic PLL loop is shown in Figure 1.

A Phase-Locked loop synchronizes a reference signal with a signal provided by an oscillator, so that they operate at the same frequency. The loop synchronizes the voltage-controlled oscillator (VCO) to the reference by comparing their phases and controlling the VCO in a manner that tends to maintain a constant phase relationship between the two. Despite the phase, which vary somewhat in some configurations, the frequency is always synchronized, otherwise the loop is said to be out of lock, [5].

The Phase-Detector (PD) compares the VCO output with the reference signal, generating a signal that changes in proportion to the phase difference. This signal then processed by the loop filter (LF), originates the VCO control signal. The loop filter can be as simple as a conductor ($u_1=u_2$), but it is usually designed to provide some advantageous response, [5]-[10]. As stated above the main difference among PLL techniques is the Phase-Detector implementation, as it will be seen next.

The techniques to be studied are, Synchronous Reference Frame (SRF-PLL), Second-Order generalized Integrator (SOGI-PLL), Enhanced PLL (EPLL) and Quadrature PLL (QPLL).

### A. SRF-PLL

A diagram of an SRF-PLL topology is represented at Figure2. A fictitious two-phase orthogonal system is obtained by introducing a phase lag of ´/2 rad in the measured single-phase voltage, (V). The output voltage components $v_{\alpha}$ and $v_{\beta}$ are described by (1),

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \begin{bmatrix} V\sin(\theta) \\ -V\cos(\theta) \end{bmatrix} \quad (1)$$

Where $V$ and $\theta$ are the peak and phase angle of the input voltage respectively.

After Park transformation $dq$ components are obtained by (2).

$$\begin{bmatrix} v_d \\ v_q \end{bmatrix} = \begin{bmatrix} v_\alpha \cos(\theta^*) + v_\beta \sin(\theta^*) \\ -v_\alpha \sin(\theta^*) + v_\beta \cos(\theta^*) \end{bmatrix} \quad (2)$$

The transformation block $\alpha\beta/dq$ uses the information $\theta^*$ about rotating reference position that is given by the PLL. When the PI is well tuned, the axis $d$ it is collinear with virtual input voltage and the quadrature component has phase error signal, so that $v_q=0$ in the steady state.

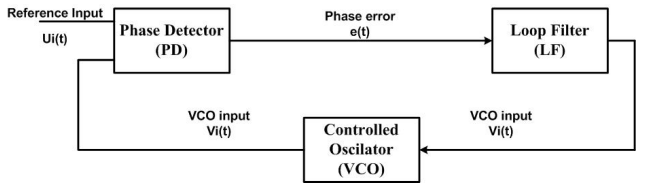


Fig. 1. General block diagram of a PLL loop.

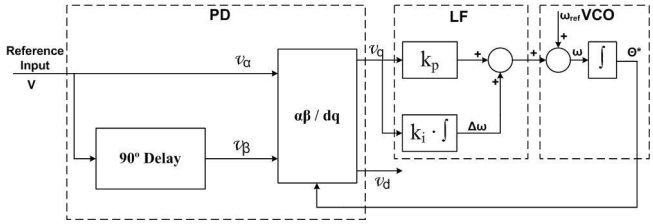


Fig. 2. Block diagram of the single-Phase SRF-PLL.

### B. SOGI-PLL

The block diagram of a PLL based on Second Order Generalized Integrator (SOGI) is shown in Figure 3. This method, like the previous, creates an orthogonal component for single-phase systems. As output signals, two sine waves, $v'$ with the same phase and magnitude as the fundamental of the input signal and $qv'$ with a phase shift of ´/2 rad, [11].

This structure as two integrators leading to a transfer function defined by (3).

$$H(s) = \frac{\omega s}{s^2 + \omega^2} \quad (3)$$

Where $\omega$ represents the resonance frequency of SOGI.

Thus the tuning of a SOGI-PLL is frequency dependent that could arise some problems related with fluctuations of the grid frequency. Consequently, adaptive tuning in respect to the resonance frequency is required.For this reason the resonance frequency value of the SOGI is adjusted by the provided frequency of the PLL, [6]-[11].

This structure presents also a gain $k$ that increases the filtering capabilities of the PLL system. If $k$ decreases, the band of the filter becomes narrower, but at the same time the dynamic response of the system becomes slower, [11].

With a SOGI structure three main tasks are preformed, they are: Generating the orthogonal voltage system; Filtering the orthogonal voltage system without delay; The structure is frequency adaptive.

### C. EPLL

The structure of EPLL is shown in Figure 4. This algorithm of the PLL is based on a frequency-adaptive nonlinear filter that is used to enhance the performance of the PD. It is actually a filter whose frequency moves based on the

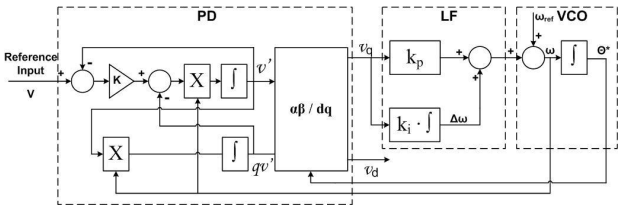


Fig. 3. Block diagram of the single-Phase SOGI-PLL.

fundamental frequency of the grid, [12].

From the input signal EPLL provides estimations of the harmonic signal, $e(t)$, the synchronized fundamental component, $y(t)$, and of the amplitude, $A(t)$, phase angle, $\boldsymbol{d}(t)$, and frequency, $\boldsymbol{\gamma}(t)$. These signals came from a relatively simple structure, but at the same time very robust and with a high level of noise and external disturbance rejection, [12]-[13].

The behavior of the EPLL system is described by the following equation system:

$$\begin{cases} e(t) = V(t) - y(t) \\ y(t) = A(t)\cdot\cos\left(\theta(t) - \dfrac{\pi}{2}\right) \\ \dot{A}(t) = k\cdot e(t)\cdot\cos\left(\theta(t) - \dfrac{\pi}{2}\right) \\ \dot{\omega}(t) = k_i\cdot e(t)\cdot\cos(\theta(t)) \\ \dot{\theta}(t) = \dfrac{\dot{\omega}(t)}{k_i}\cdot k_p + \omega_r(t) \end{cases} \quad (4)$$

Three parameters, $k$, $k_p$ and $k_i$, control the accuracy and speed of convergence of the EPLL system. Parameter $k$ dominantly controls the speed of the amplitude convergence and parameters $k_p$ and $k_i$ the rates of convergence of phase and frequency, respectively. The dynamic of the variables are coupled and they mutually affect each other. A tradeoff between the desired dynamic and the steady-state error should be accomplished when choosing the gain values.

### D. QPLL

The QPLL generates the fundamental component based on estimations for the in-phase and quadrature amplitudes as well as frequency and phase variations, [10]. The QPLL structure makes use of a first-order optimization algorithm, the gradient--descent method, to estimate its parameters. Further analysis regarding the mathematical behavior of the QPLL can be found in [14].

The QPLL considers a sum of two in-phase and quadrature-phase components for its output. The equation system for the QPLL can be derived by (5).

$$\begin{cases} e(t) = V(t) - y(t) \\ y(t) = k_S(t)\cdot\sin(\theta(t)) + k_C(t)\cdot\cos(\theta(t)) \\ \dot{k}_S(t) = 2\mu_S\cdot e(t)\cdot\sin(\theta(t)) \\ \dot{k}_C(t) = 2\mu_C\cdot e(t)\cdot\cos(\theta(t)) \end{cases} \quad (5)$$

The error signal, $e(t)$, is used to adaptively estimate the quadrature and in-phase amplitudes, $k_s(t)$ and $k_c(t)$, as well as the phase, $\boldsymbol{d}(t)$. Three gains control the behavior of the QPLL. The parameters $\boldsymbol{\varepsilon}_s$ and $\boldsymbol{\varepsilon}_c$ affect the in-phase and quadrature amplitudes, respectively. Parameter $\boldsymbol{\varepsilon}_f$ is directly related with the frequency, $\boldsymbol{\gamma}(t)$. If $\boldsymbol{\varepsilon}_s = \boldsymbol{\varepsilon}_c = \boldsymbol{\varepsilon}_f$ it is possible to simplify the structure, as stated at [14].

The sophisticated PD in QPLL methods allows estimating the phase angle time derivative of the input signal, resulting in more accurate values for the frequency, given by (6).

$$\omega(t) = \frac{d\theta(t)}{dt} \quad (6)$$

Another advantage in this structure is the lack of nonlinear dependency of the error signal to the phase difference, thus the VCO receives a signal equal to the phase variations.

The QPLL is expected to have high performance and fast convergence rates, [10, 12, 14].

Figure 5 shows a block diagram of the single-phase QPLL method.

### E. Computational requirements

PLL systems are based on mathematical relations, an appropriate structure to be implemented in Digital Signal Processors for further interaction with converters.

For a correct behavior of the system is of critical importance to use processors able to give fast and accurate results. Since algorithms are platform-independent, follows a generalized analysis to give a simple and quick reference method for choosing the correct implementation system.

To analyze an algorithm is to determine the amount of resources (such as time and storage) necessary to execute it. The growth rate in complexity of algorithms can be described by the number of simple operations performed, e.g., additions

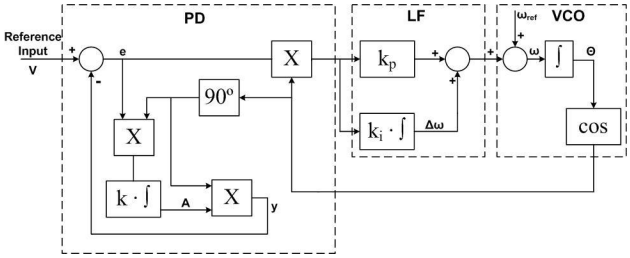


Fig. 4. Block diagram of the single-phase EPLL.

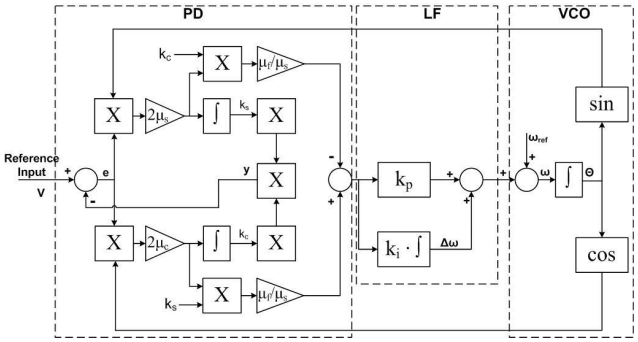


Fig. 5. Block diagram of the single-phase QPLL.

and multiplications. Referring to the PLL algorithms is possible to describe all the mathematical chain with simple operations by means of series expansions, e.g., Taylor Series for trigonometric functions.

Table I reflects this analysis for each of the abovePLL methods discussed. The analysis is only regarding to the PD and VCO blocks, the LF is interchangeable.

## III. PLL LINEARIZATION AND CLOSED LOOP ANALYSIS

The PLL is a closed-loop system like the one represented before in Figure 1. This kind of control systems has many advantageous regarding to open-loop systems. They reduce the sensitivity to parameter variation, leading to robust control and increased performance. The challenge in the tuning process of a closed-loop system is to have an accurate description of all the elements in the loop in order to induce a behavior or a working period where the feedback control can completely or partially remove the effect of disturbance signals while maintaining good transient response, [15].

Look at the classical PLL loop, the SRF-PLL, the PD and VCO elements are described by the equations (1) and (2). Once the *q* component as information regarding the phase error will be the component with more interest to the analysis and the *d* component as referred previously, can be neglected.

Assuming $\theta^*$ like:

$$\theta^* = \theta' - \frac{\pi}{2} \tag{7}$$

The component *q* can be simplified to:

$$V_q = V \cdot \sin(\theta - \theta') \tag{8}$$

Where $\theta'$ is equal to the input phase angle with some little variation. This way it is possible to eliminate the oscillatory component of $V_q$ and therefore reduce the analysis to a linear system. Both Phase Detector and Voltage Control oscillator can be seen as gain multipliers, $K_{PD}$ and $K_{VCO}$ respectively, so a conventional PLL loop will be like the one represented in Figure 6.

TABLE I
PLL TECHNIQUES ALGORITHM COMPLEXITY.

| PLL | Add/Sub | Mul/Div | Complexity |
|---|---|---|---|
| SRF-PLL | 5 | 13 | 2 |
| SOGI-PLL | 8 | 14 | 3 |
| EPLL | 3 | 8 | 1 |
| QPLL | 6 | 16 | 4 |

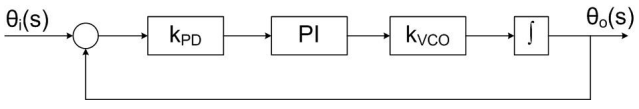


Fig. 6. Linear PLL loop.

The most common filter in PLL loops is the Proportional Integral Filter, [6]-[10], which is well defined in the literature, [15]. If $K_{PD}=K_{VCO}=1$ the transfer function of the linearized PLL is:

$$H(s) = \frac{\theta_i(s)}{\theta_o(s)} = \frac{K_p \cdot s + K_i}{s^2 + K_p \cdot s + K_i} \tag{9}$$

Where the damping ratio and the natural frequency are:

$$\xi = \frac{K_p}{2 \cdot \sqrt{K_i}} \tag{10}$$

$$\omega_n = \sqrt{K_i} \tag{11}$$

$K_p$ and $K_i$ are the proportional gain and the integral gain respectively.

This second order system has all the poles in the left-half part of the complex plane, which is a necessary and sufficient condition for a stable system. Thus the control design should only care about good transient response and good noise rejection together with low overshoot and low settling time. For a system like the PLL the following design criteria should be met, [15]-[16]:

- $\xi$ å 0,7, for good transient response;
- Low $\omega_n$, for narrow bandwidth and improved noise rejection, to obtain purely sine waves at the output even in the presence of harmonics.

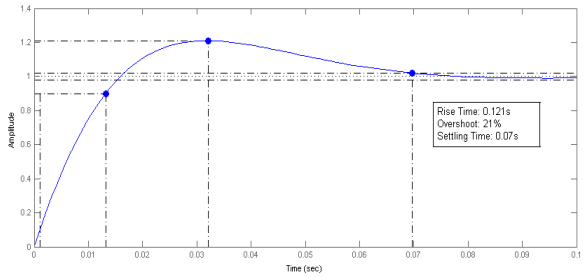


Fig. 7. Step response of the classical PLL system.

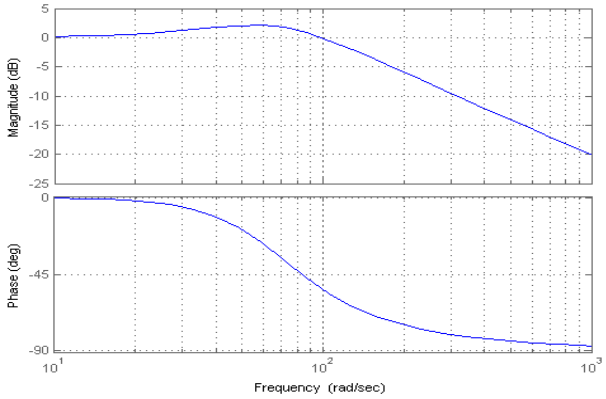


Fig. 8. Bode plot of the classical PLL system.

Especial care must be taken when choosing a very narrow bandwidth, because the lock range could be lost. The PLL lock range is defined as the maximum initial frequency deviation between reference input and VCO output, which will still cause the PLL to get locked in a single beat, it is approximately equal to the natural frequency $\omega_n$, [15].

Having this design criteria in mind and after setting the parameters it is possible to plot the step response as well as the bode plots for the system to verify the correct design. The plots are represented in Figures 7 and 8.

As expected the system shows good transients as well as low overshoot. The system has narrow bandwidth that indicates high noise rejection and the system as the same behavior as a low pass band filter, rejecting frequencies above 70Hz. High stability and robustness are obtained as a consequence of the high phase and gain margins.

## IV. Simulation Results

Performance of different synchronization techniques has been tested considering different disturbances: Frequency and voltage variations, harmonic disturbance immunity. At the end, a table with the performance parameters of each method is discussed.

These results were obtained using Simulink® platform to simulate each of the synchronization methods. All the simulations have a time interval of 1s, which is proved to be enough to observe the desired characteristics.

### A. Frequency Variations

To test the behavior and dynamics of the PLL in case of frequency variations, a reference that imposes a negative variation of 10% followed by a positive variation of 10% has been considered. The results are presented in Figures 9 to 12.

The SRF-PLL and the EPLL presents relevant frequency oscillation. Although, for the EPLL, the behavior could be improved if the PI controller is correctly tuned, because in this method the Integral Gain controls the convergence rate of the frequency. The SOGI-PLL and the QPLL present a good tracking capability. The SOGI-PLL has a constant ripple even when the reference stabilizes; contrariwise the QPLL in a few milliseconds is following the reference without any deviation.

### B. Voltage Variations: Voltage Sag

For this experiment, voltage sag of 20% of the grid is used to evaluate the PLL performance. The initial behavior, such

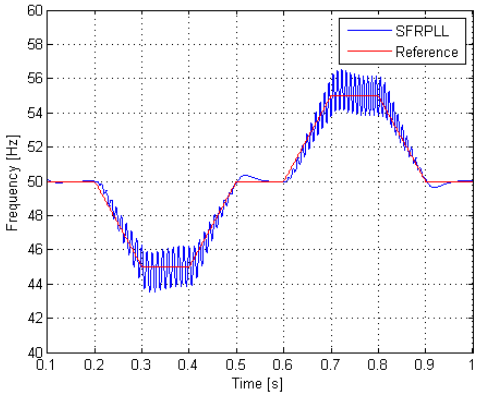


Fig. 9. SRF-PLL Frequency variations behavior.

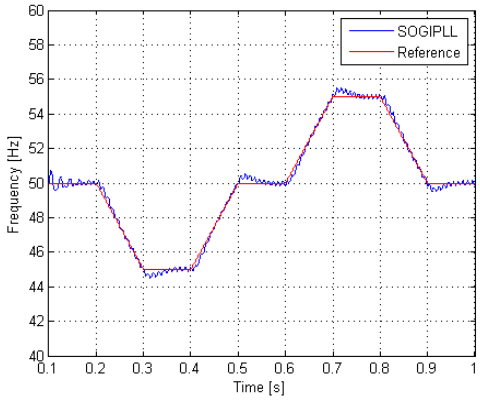


Fig. 10. SOGI-PLL Frequency variations behavior.

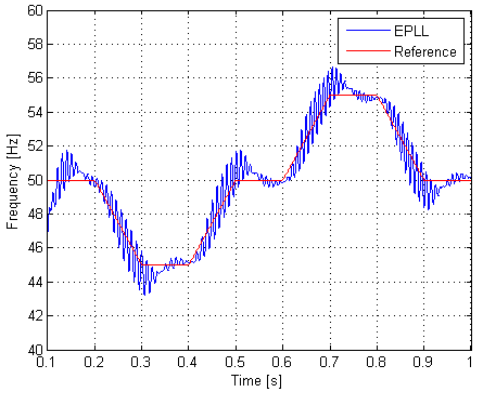


Fig. 11. EPLL Frequency variations behavior.

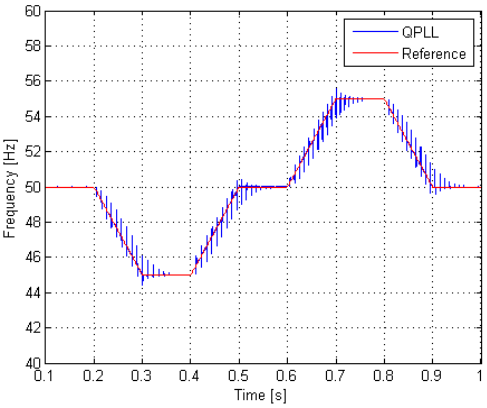


Fig. 12. QPLL Frequency variations behavior.

as overshoot, settling time and oscillations, can also be analyzed in this test.

All the methods are fast and accurate to calculate the amplitude of the grid. The SOGI-PLL method exhibits some ripple whereas the others not. The initial behavior of the QPLL and the SRF-PLL are fast, with no overshoot and no oscillations, both methods have very good dynamics. On the other hand, SOGI-PLL and EPLL presents high oscillations and large settling times.

These results can be analyzed in Figures 13 to 16.

### C. *Effect of Harmonic disturbances*

To analyze this behavior a grid signal distorted by harmonics is used. The harmonic disturbance applied is accordingly to the Portuguese Standard EN50160, [18].

This analysis is restricted only to steady state mode, whereas the results can give more valuable information.

The SRF-PLL and the SOGI-PLL are highly affected by harmonics, although the SOGI-PLL can perform some filtering and reduce the effect of harmonics. The EPLL and the QPLL present a small steady state error in amplitude estimation. Both methods have good filtering characteristics. The QPLL has the best performance in reducing the harmonic disturbance. Both frequency and amplitude estimation have little error.

These results are mirrored in Figures 17 to 20.

### D. *Performance parameters*

Table II shows some of the parameters used to evaluate the overall performance of a PLL. The lock range, that is the frequency range around the nominal VCO frequency in which the loop can acquire lock within one cycle, shows that the SRF-PLL will continue locking the input signal even when this signal is affected by noise. The EPLL and the QPLL have a small frequency range, which indicates that these two methods must have a frequency estimator in the VCO. For the SOGI-PLL, because it uses the same frequency in the VCO and in the PD, the results obtained for the lock range are not suitable for analysis.

From the table, it is possible to see that the QPLL is the faster method. This method locks in 25ms and enters in the error band in 20ms. The error band defined is 1% of the frequency and 15% of the amplitude, the same error band stated at [18].

To complete this analysis is important to say that, only the SOGI-PLL method shows steady state error, whereas the

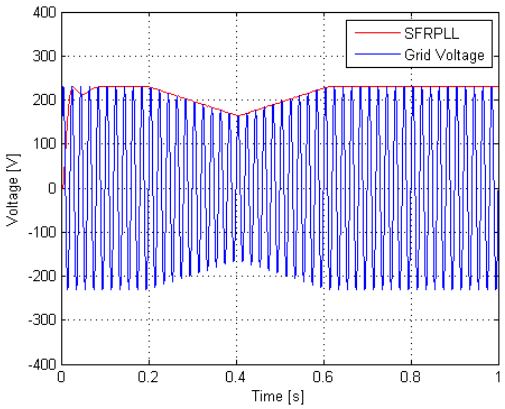


Fig. 13. SRF-PLL Voltage variations behavior.

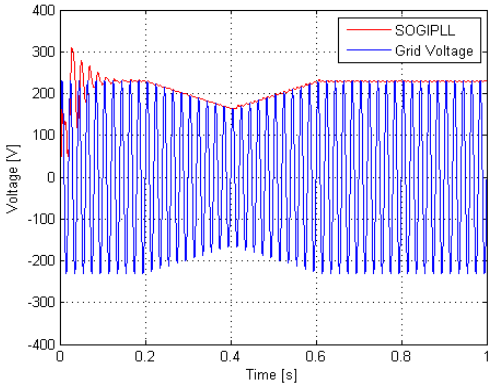


Fig. 14. SOGI-PLL Voltage variations behavior.

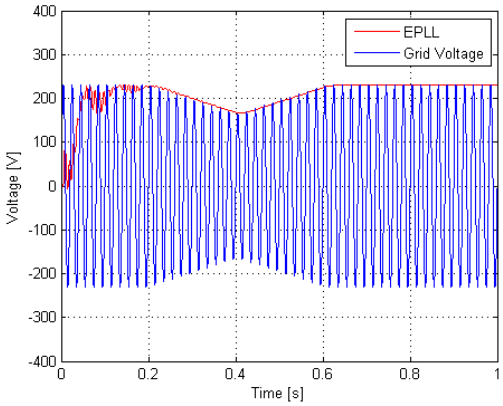


Fig. 15. EPLL Voltage variations behavior.

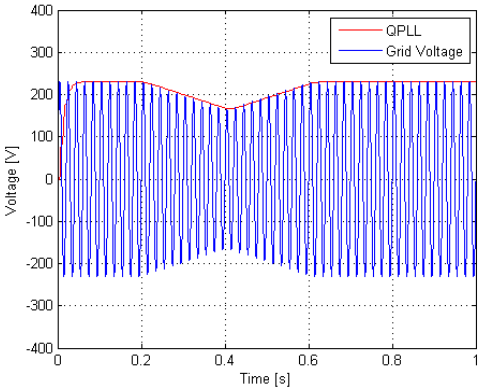


Fig. 16. QPLL Voltage variations behavior.

other methods have no error. Even though, the steady state error in SOGI-PLL can be easily neglected and lowered with appropriate filtering.

*E. Discussion*

All the methods have high complexity and should be implemented in systems with high frequency and memory. But if there is some sort of limitation regarding the processor or memory, the first method to be chosen is the EPLL. Is the method with fewer operations and consequently with the lower level in complexity, 1.

In the case of frequency variations, the SRF-PLL has a relevant frequency oscillation, while the SOGI-PLL and the QPLL have short transients with small oscillation. The EPLL, have big oscillation, although this behavior results from an inappropriate loop tuning, which indicates that the loop for this method cannot be generalized.

Considering voltage falls, all the PLLs rapidly follows the amplitude variation, with the EPLL being the method with slower transients. In this test the SOGI-PLL presents a

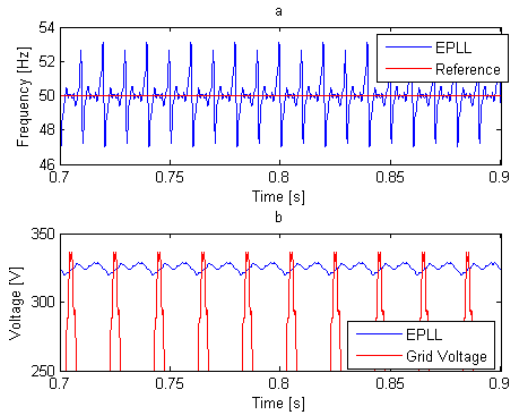


Fig. 19. EPLL Harmonic Distortion. a) Frequency; b) Voltage.

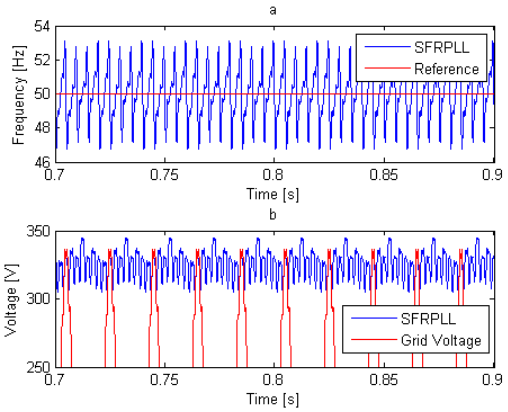


Fig. 17. SFR-PLL Harmonic Distortion. a) Frequency; b) Voltage.

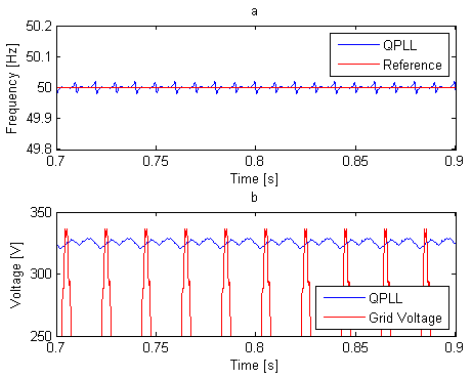


Fig. 20. QPLL Harmonic Distortion. a) Frequency; b) Voltage.

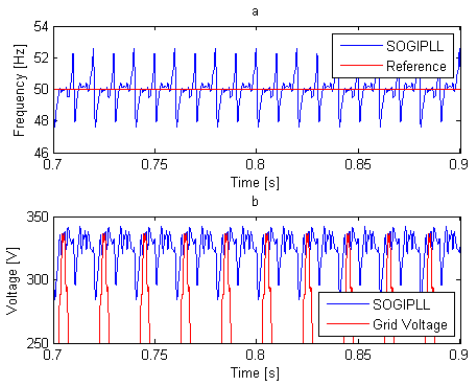


Fig. 18. SOGI-PLL Harmonic Distortion. a) Frequency; b) Voltage.

TABLE II
PERFORMANCE EVALUATION OF PLL METHODS.

| PLL Method | Lock Range (Hz) | Lock Time (ms) | Settling Time (ms) | Overshoot | Frequency estimation Error (with Harmonics) | Amplitude Estimation Error (with Harmonics) |
|---|---|---|---|---|---|---|
| SRF-PLL | 43 ï 58 | 90 | 80 | 3,2 % | 6,2 % | 4,7 % |
| SOGI | X | 130 | 125 | 15,32 % | 5,1 % | 3,9 % |
| EPLL | 45 ï 54 | 180 | 170 | 33 % | 6,0 % | 3,3 % |
| QPLL | 49 ï 51 | 25 | 20 | 0 % | 0,1 % | 2,9 % |

considerably overshoot and the EPLL the larger settling time.

For an input signal disturbed by harmonics, the QPLL and the EPLL presents a high filtering capability, with the frequency estimation given by the QPLL being almost unaffected. The SRF-PLL is heavily affected by harmonics revealing is insufficient filtering capability.

All the methods have some specific advantage. The SRF-PLL despite is poor filtering capabilities present low complexity and large Lock-Range. The SOGI-PLL has short transients and small errors in following oscillating signals, although even when the signals are fixed, it shows a small steady state error. The EPLL, have good filtering capabilities and a good Lock-Range, but the performance of this method is limited to a proper loop tuning. The QPLL is the most complex method and presents a short lock range, despite that, is the faster method, with very low errors and high filtering capabilities.

## V. Conclusion

In this paper an overall comparison of different phase locked loop techniques is performed. All the methods are studied, in a computational simulation environment, regarding the connection to a single-phase grid.

The objectives proposed at the introduction were accomplished. For the analysis conducted two methods stand out among the others: SRF-PLL and QPLL. The SRF-PLL for its simplicity and ease of implementation and the QPLL for its high filtering capabilities and performance.

Further developments should predict high order algorithms to enhance performance.

## VI. References

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