An Impulse-Radio UWB Transmitter for Short-Range Communication Systems

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***Abstract*—This work addresses the design of an impulse-based ultra-wideband transmitter targeting short-range radio systems in the 3–10 GHz band. In this paper we describe the complete transmitter at circuit level, from baseband data input up to the antenna interface. To ensure the output signal fits within the FCC-UWB spectrum mask, the transmitter comprises nearly-independent tuning structures and supports multi-modulation formats. The proposed circuits have been designed in a mixed-signal/radio-frequency CMOS 90-nm process. Post-layout simulation results are presented, including several process corners, which further demonstrate the ability of the transmitter to proper compensate for parameter deviations.**

I. Introduction

The regulation of the ultra-wideband (UWB) spectrum by the Federal Communications Commission (FCC) [1] gathered remarkable interest in new technologies for low-power wireless communications [2]. Two different approaches have been followed in the deployment of UWB-based systems, one relying on orthogonal frequency-division multiplexing (OFDM), and the other employing impulse-radio (IR) techniques. Essentially, the former targets high data-rates, while the latter is particularly suited for short-range communication systems [3]. In this last case, the design of energy-efficient IR transmitters favors numerous battery-operated applications where power is a scarce resource. When compared to other low-power narrow-band alternatives, IR-UWB has been shown to be more efficient due to typically reduced energy consumption in the transmitter hardware [4]. With simplified physical layers, power consumption tends to μ-Watt levels, which further enables power-harvesting techniques [5]. The pulses can be realized in the 3.1–10.6 GHz band with extremely low radiation levels (below -41.3 dBm/MHz). This enables the implementation of highly-integrated solutions using CMOS processes. As a result, the UWB application range widens from military radar to wireless personal and body area networks (WPANs and WBANs, respectively), imaging systems, and sensor networks.

Lately, some interest has also been drawn on IR-UWB technologies for medical applications [6]–[8]. In fact, for long-time operation, impulse radio presents some advantages for centimeter-range communications when compared to typical Medical Implant Communication Services (MICS) [8]. This is particularly attractive for short-range telemetry in biomedical systems where wired links are undesirable due to the risk of infections. Some examples include neural recording implants [9], retinal implants, capsule endoscopes [7], among other related in-body or wearable monitoring systems [10]. In some of these applications, the amount of data to be transmitted can be considerably large [11]–[13]. However, high data-rate communication can compromise energy efficiency in IR-UWB systems and increase sensitivity to process variations. As such, tuning circuits are needed to ensure compliance with the FCC spectrum mask [14]–[16]. In this paper, we present the CMOS design of an IR-UWB front-end using the architecture depicted in Fig. 1. To reduce the dependence on process corners, the proposed architecture incorporates several tuning schemes as nearly-orthogonal processes for adjusting amplitude, bandwidth and central oscillating frequency.

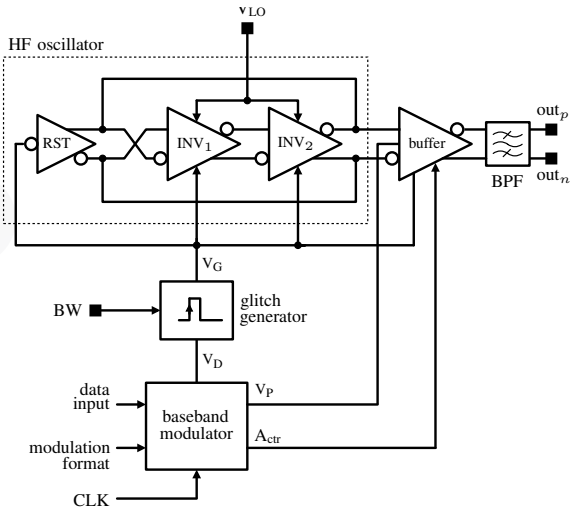


Fig. 1: Proposed front-end IR-UWB architecture.

II. Proposed Architecture

The architecture of an IR-UWB is essentially defined by the pulse generation approach. Carrier-less techniques can be used to produce sub-nanosecond pulses without requiring any local oscillator. Most approaches rely on monocycles synthesized with delay elements [17]. Although this method aims at fully-digital implementations, a pulse-shaping circuit is most of the

times required at the transmitter output. Moreover, since pulse shaping is typically implemented through passive devices, this approach only allows for delay adjustments. This represents a limiting factor in assuring the FCC compliance of the synthesized pulses.

Alternatively, carrier-based techniques extend the flexibility to proper calibrate the sub-nanosecond pulses [18]. The transmitter architecture described herein relies on this approach. Fig. 1 shows the circuit blocks that comprise the proposed front-end system, namely a baseband modulator, glitch generator, high-frequency (HF) oscillator (INV_1, INV_2, and RST), output buffer and bandpass filter (BPF). This architecture provides nearly-independent calibration schemes for the UWB pulses to fit within power-spectral-density (PSD) mask as regulated by the FCC.

The peak PSD of the transmitted pulses, which must be lower than -41-dBm, can be adjusted using the voltage signal A_{ctr} at the output buffer. Additionally, the central frequency of the pulse spectrum can be shifted through proper calibration of the V_{LO} input at the high-frequency oscillator. The pulse bandwidth is imposed at another circuit block, that is the glitch generator. By regulation of the BW signal, the pulse length produced by the glitch generator can be adjusted. This has immediate impact on the bandwidth of the transmitted pulses.

These three ideally-orthogonal mechanisms can still be complemented at data-encoding level. The present transmitter is designed to attain 1-Gbps data rate, but the required processing gain is essentially dictated by the receiver performance in collecting the transmitted bits. Hence, pulse repetition can be employed during data encoding and set accordingly with the required data rate. In the proposed transmitter, the data rate is defined at baseband. At the modulator input, the baseband data uses a clock signal (CLK) as its time reference. Additionaly, the desired modulation scheme can be selected at the modulator block, which is responsible for defining how the CLK and data signals are applied to the IR-UWB front-end.

A. Baseband modulator

To accommodate for channel diversity, the front-end supports different modulation formats. The present architecture is designed to support binary phase-shift keying (BPSK), pulse-position modulation (PPM), and on-off keying (OOK). As shown in next sections, the chosen approach for the implementation of a multi-modulation scheme has no significant impact on design complexity.

Referring to Fig. 1, BPSK is accomplished by connecting the data input directly to the buffer (V_P), and with the CLK signal driving the glitch generator to synchronize data output. Through the voltage level of V_P, high or low, the pulses can present opposite phases. For PPM, V_P is kept at a constant voltage. The data input imposes the required delay driving the glitch generator. Similarly, the pulses for OOK modulation are accomplished by connecting the data input directly to the glitch generator.

B. Glitch generator

The glitch generator is responsible for the activation of subsequent transmitter blocks. A glitch is generated for each bit to be transmitted, triggered by positive-edges of return-to-zero pulses from its input. During this time interval, the ring-oscillator is activated, and at the end of the glitch, the reset block (RST) forces the ring-oscillator nodes to a well-known state.

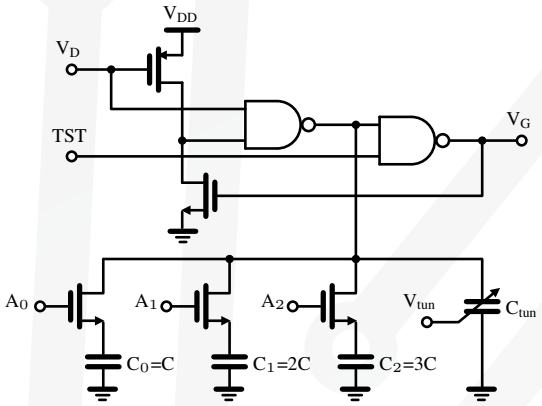


Fig. 2: Glitch circuit with pulse-length calibration.

Fig. 2 shows a circuit adopted from [19]. A test signal (TST) is added to deactivate the glitch generator and allow for independent calibration of the ring-oscillator operating frequency. The pulse length can be adjusted through a binary-weighted capacitance array. The signal BW depicted in Fig. 1 corresponds to the digital word A_2–A_0 associated to the binary weighted capacitance array C_2–C_0. The input V_{tun} controls the varactor C_{tun} to provide fine tuning for the desired glitch length. With this adjustment, it is possible to calibrate the rising and falling edges of the first NAND gate. Fig. 3 shows the calibration obtained with different digital control words and tuning voltages.

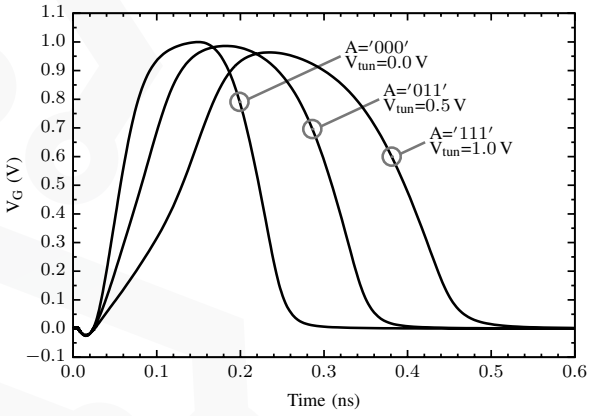


Fig. 3: Glitch calibration through the capacitance array.

C. High-frequency oscillator

The proposed high-frequency ring oscillator is depicted in Fig. 4. A fully-differential topology is preferred to improve rejection of power-supply and substrate coupling interferences. The oscillator comprises two inverters in a cross-coupled configuration with regenerative feedback, which allows for a higher oscillation frequency. A reset circuit is included as well to force fast damping when the glitch-generator voltage V_G goes into low state.

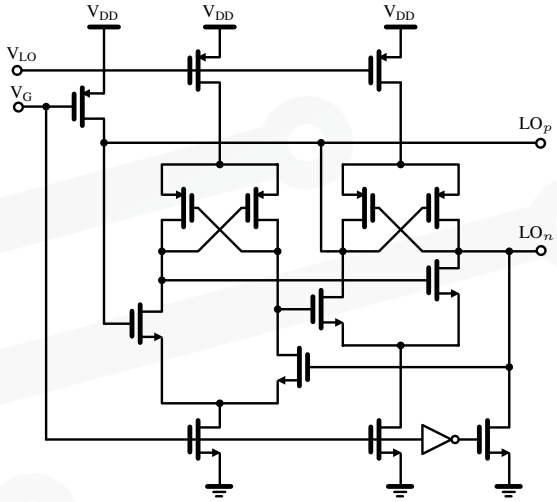


Fig. 4: High-frequency oscillator.

The voltage V_{LO} controls the current drawn from power supply and, consequently, the oscillation frequency. Fig. 5 shows the oscillating frequency tuning-range controlled through the V_{LO} input. Different capacitance values are used to represent the influence of the output load. Optimizing transistor ratios, this configuration allows relatively low-power dissipation at high-frequency regimes. The central frequency is chosen at the mid-range of the FCC mask, between 5 and 6-GHz.

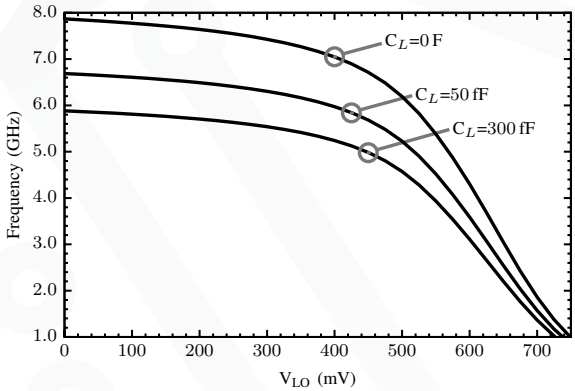


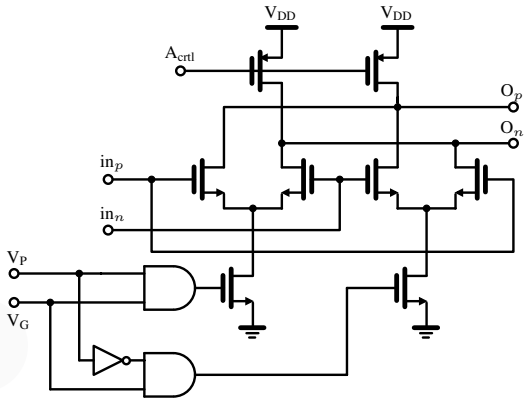
Fig. 5: Oscillator output frequency as a function of V_{LO}.

D. Output amplifier and pulse shaping

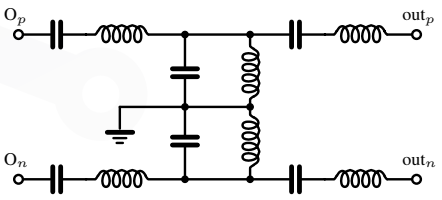
The output amplifier is shown in Fig. 6a. Amplitude control is provided by the A_{ctr} voltage, which defines the current drawn at each differential stage. This plays an important role since for different modulations, e.g. PPM and OOK, the voltage A_{ctr} has to be properly regulated at the baseband modulator to comply with the peak PSD[1].

Another interesting feature of the proposed buffer is that, depending on the voltage V_P imposed by the modulator, the output polarity is defined – this is particularly useful for the BPSK modulation.

Pulse shaping is implemented through the balanced tee-section shown in Fig. 6b. Simulations performed on the bandpass filter allowed to define its bandwidth and central frequency, taking also into account the need for a fast transient response. As a result, to comply with the FCC mask, the filter can be designed with inductances in the range of 1 to 5-nH with unloaded quality factors above 15, and 100 to 400-fF for the capacitors. This enables full integration of the passive devices in CMOS technology. The filter was designed with on-chip circular inductors and metal-insulator-metal capacitors. It provides a 6.5-dB bandwidth at -10-dB with an insertion loss of 5-dB at central frequency of 6-GHz.



(a)



(b)

Fig. 6: Circuits proposed for the (a) output buffer and (b) pulse-shaping filter.

[1] In fact, under nominal conditions, each modulation has its own A_{ctr} voltage value due to different power densities. Hence, this needs to be taken into account at the baseband modulator upon modulation selection.

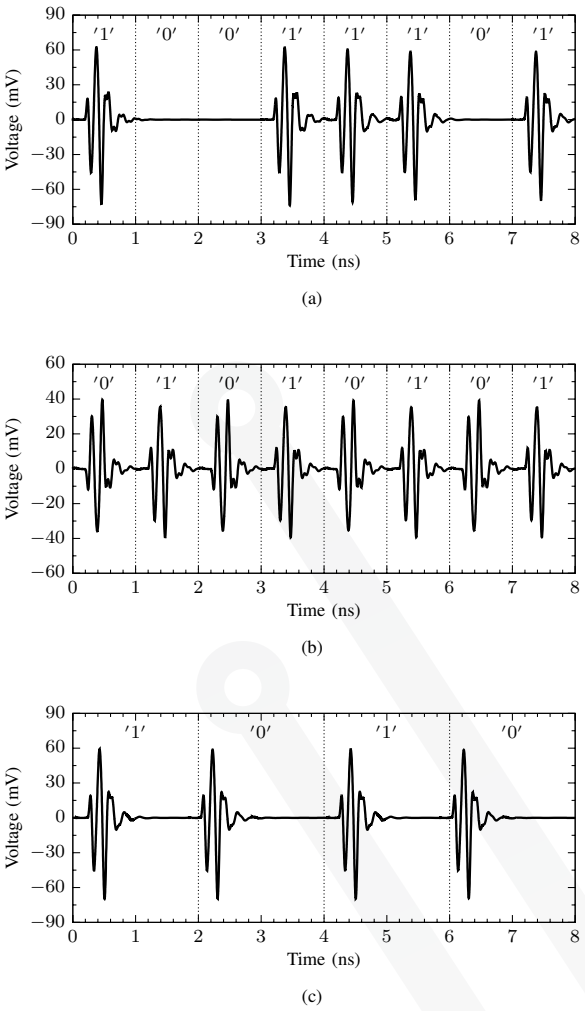


Fig. 7: Time-output simulation waveforms for the IR-UWB modulation formats supported in the present architecture – (a) OOK, (b) BPSK, and (c) PPM.

III. Simulation Results

The proposed UWB transmitter architecture has been designed in a mixed-signal/radio-frequency CMOS 90-nm process with low-κ dielectric and 1.2-V triple-well MOS devices. All post-layout simulations have been performed using SpectreRF from Cadence Design Systems with BSIM3v3 device models. Calibre from Mentor Graphics was used for layout parasitic extraction (PEX).

In order to fully test the proposed UWB architecture, a set of post-layout simulations were performed applying different types of modulations to the transmitter. Fig. 7 depicts the simulation results under typical operating conditions. As shown, good symmetry can be noticed for the pulses. For both OOK and BPSK modulations the bit period was held at 1-ns, which translates into a 1-Gbps data rate. Fast transient response is achieved for any of the proposed modulations, although the data rate in the PPM has been made considerable lower (500-Mbps) to prevent pulse overlapping.

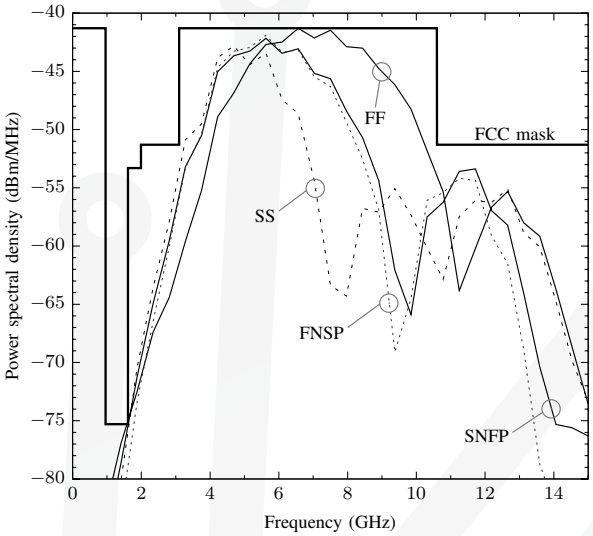


Fig. 8: Pulse PSD for post-layout simulation of CMOS process corners.

The reliability of the design was also put under test with post-layout simulations of different types of process deviations. Fig. 8 shows the results for a 1-Gbps BPSK signal with four different CMOS process corners: slow-slow (SS), fast-fast (FF), slow-N fast-P (SNFP), and fast-N slow-P (FNSP). The proposed tuning circuits were used to correct subsequent parameter deviations – the results presented were obtained after calibration. As seen, all process deviations considered can be properly adjusted so that the respective PSD falls within the FCC UWB spectrum mask.

Process deviations have also a great impact on overall power consumption. For the case of 1-Gbps BPSK modulation, energy per pulse is about 14.6-pJ for nominal conditions. When considering process deviations, and without any adjustments, this value can go from 13.2 to 19.6-pJ for SS and FF corners respectively. Nevertheless, the required compensation is limited to the way process corners affect side lobes of the pulse PSD. As such, proper adjustments have little effect on efficiency – following UWB pulse calibrations, the same corners respectively lead to 13.3 and 18.9-pJ. This is also related to the way power is distributed among circuit blocks. For typical operation, most of the power consumption takes place at the HF oscillator (57%) and glitch generator (41%).

The layout of the transmitter is shown in Fig. 9. It occupies solely 0.46-mm^2 with bond-pads. All components are integrated, including the six inductors.

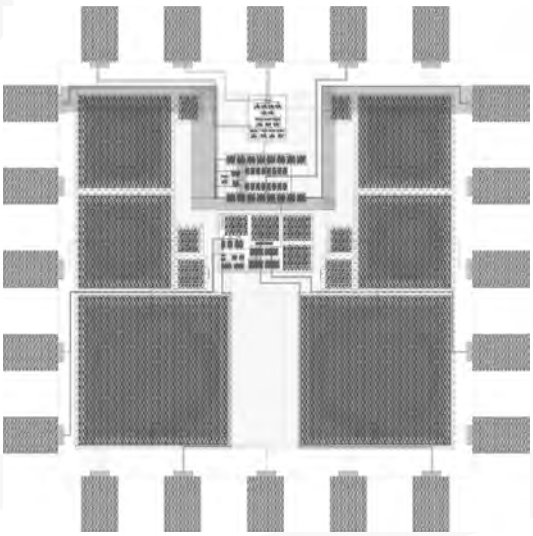


Fig. 9: CMOS design layout of the proposed transmitter (675×675-μm^2).

IV. Conclusion

In this work, an IR-UWB transmitter front-end has been presented. Without a significant increase in design complexity, the proposed solution provides a flexible way of UWB transmission using different modulation schemes, namely BPSK, PPM, and OOK. High data-rates can be accomplished for any of these modulations. Furthermore, the proposed architecture allows for the adjustment of the output pulse waveforms in order to obtain FCC-compliant spectrum masks. Center oscillator frequency, amplitude, and pulse length can be adjusted almost independently. The implementation of the circuits comprising the proposed architecture has been presented for a fully-integrated 90-nm CMOS design. Post-layout simulation results demonstrate that the proposed approach can effectively compensate for parameter deviations to obtain FCC-compliant pulse waveforms.

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