BIST Design for Analog Cell Matching

Cândido Duarte, Henrique Cavadas, Pedro Coke, Luís Malheiro, Vítor Grade Tavares, and Pedro Guedes de Oliveira
INESC TEC (formerly INESC Porto) and Faculty of Engineering, University of Porto
Microelectronics Students' Group, Faculty of Engineering, University of Porto
Campus da FEUP, Rua Dr. Roberto Frias, 378 4200–465 Porto, Portugal
Email: candidoduarte@fe.up.pt

***Abstract*—This work addresses a built-in self-test methodology for circuit cell identification under specific matching conditions. The proposed technique is applied to the CMOS realization of a reduced-KII network, which is a system model of the biological olfactory cortex. This model behaves as an associative memory, a useful tool for information and adaptive processes.**

Based on a mixed-signal approach, the test strategy makes proper use of the circuits comprising the network structure, and provides self reconfiguration as well. Both testing procedures and design of essential building blocks are described in this paper. Simulation results are presented for a reduced-KII network comprising 128-cells, sequentially tested for matching in terms of offsets and their dynamic performances.

***Keywords*-adaptive processes; design for testability; matching algorithms; mixed-signal BIST; neuromorphic circuits;**

I. Introduction

The implementation of analog computational systems often relies on simple processing building-blocks that are repeated in a network structure. With networks featuring noticeable cell interaction, inherent asymmetries or parametric faults in analog cells may impose some limitations on global performance. Regarding artificial neural networks, robustness to fault tolerances is accomplished by redundancy and learning, though only to a certain degree. In principle, large networks render higher redundancy. However, in many situations the size is limited, either due to the network model such as the case study presented in this paper, or to mitigate the mean/variance dilemma [1].

Establishing a built-in self-test (BIST) procedure, based solely on local deterministic methodologies, does not represent an efficient test approach for analog processing networks. The information is distributed along the network structure, often with redundancy, and requires less typical methods to cover fault detections in an effective manner [2]. Hence, existent BIST techniques applied to basic building circuits, such as switched-current (SI) memories [3]–[5], capacitor arrays [6], and analog filters [7], can be inefficient as a test procedure for analog computational networks. Global methods are required for parametric-faults detection, which should focus on system performance rather than component level, and make adjustments accordingly.

This work presents a methodology for offline matching-detection and its implementation as a test procedure for reduced-KII (RKII) networks [8], [9]. Since a great part of the RKII circuitry is common to other neural networks, the test methodology can be readily extended to those networks.

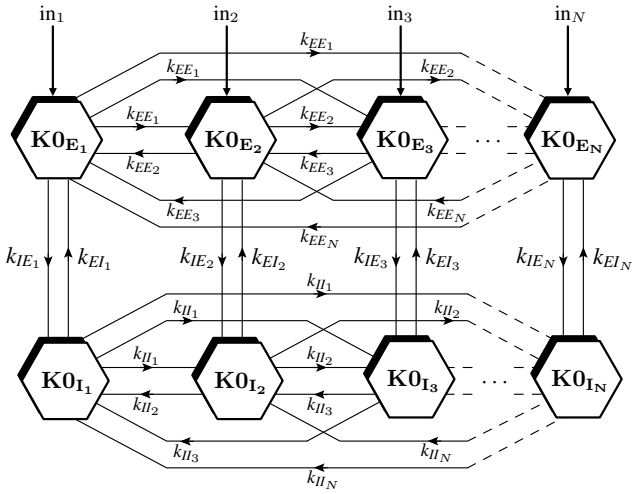


Fig. 1: N-channel reduced-KII network.

The proposed technique aims to determine which cells in the network present most similar performance. The resulting analog circuitry overhead for testing is very limited, with part of the testing resources reused from the actual network circuits.

A. RKII Network

Katchalsky sets (K0) are the simplest form of a more complex dynamical model proposed by Walter Freeman to explain olfactory cortex behavior in mammals [8], [10]. Freeman departs from a single neuron approach to model networks from a population of neurons – K0, which represents the fundamental building block, or processing element. It embodies a second-order linear equation followed by a static, non-symmetrical sigmoid function, raised from biological evidence. High-order behavior is accomplished by interconnecting these elements in a well-defined hierarchical procedure. The interconnection of two K0s, with either positive ($K0_E$ denoting excitatory) or negative ($K0_I$, inhibitory) weights, forms a KI set. By interconnecting one excitatory KI with an inhibitory KI, a KII set is built. This procedure is followed to accomplish higher order levels, namely KIII and more. Interconnecting a given number of sets embeds a network. Fig. 1 shows an example of a KII network set. This network represents the olfactory bulb in Freeman's olfactory model and brings together a series of properties attractive for engineering purposes. A KII set,

978-1-4673-0697-3/12/$31.00 ©2012 IEEE

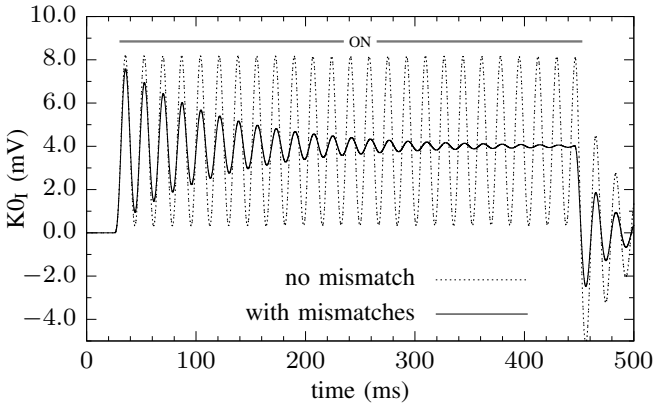


Fig. 2: Impact on the RKII oscillating behavior due to dynamic mismatches.

when well parametrized, is an oscillator with fixed frequency, whereas the energy is controlled by an external input. Therefore, a network of KII sets (Fig. 1) topologically represents a network of coupled oscillators. Coupling unbalancing, performed according to some correlation with the input vector, results in output-vector oscillating patterns with amplitude values that are related to the input information. This is a typical associative memory behavior, such as that of the Hopefield net [11], with a difference, the stable recalled pattern is not a fixed-point in the phase-plane but a limit-cycle, demanding now much less energy when jumping from pattern to pattern.

Fig. 1 depicts in fact an RKII representation of a KII network. It uses less resources and maintains the KII properties for large number of channels (inputs – oscillators). The individual response of an RKII cell is not absolutely critical for system operation, however relative responses are. As illustrated in Fig. 2, if a number of cells in the network present too dissimilar natural responses, coupling may be preempted therefore making the network impractical. This is the motivation behind the BIST design for this network in particular.

II. BIST Approach

Classical test procedures for analog circuits rely on meeting some set of specifications. Such procedure can be cumbersome and expensive due to the elaborate testing infrastructures needed. Several authors have mitigated this problem, for example by reducing the number of specification test-sets [12], [13]. The BIST approach in this work fits within this category but, for reasons previously dissected, the global performance is addressed instead of local hardware elements (e.g. individual amplifiers).

As earlier referred, the proper RKII network operation demands a certain degree of similarity between cells. The goal of the proposed BIST methodology is to classify the largest group of cells having similar dynamics, within a predefined tolerance. Fig. 3 shows a possible probability density function (PDF) representation for a given figure-of merit (FOM) along

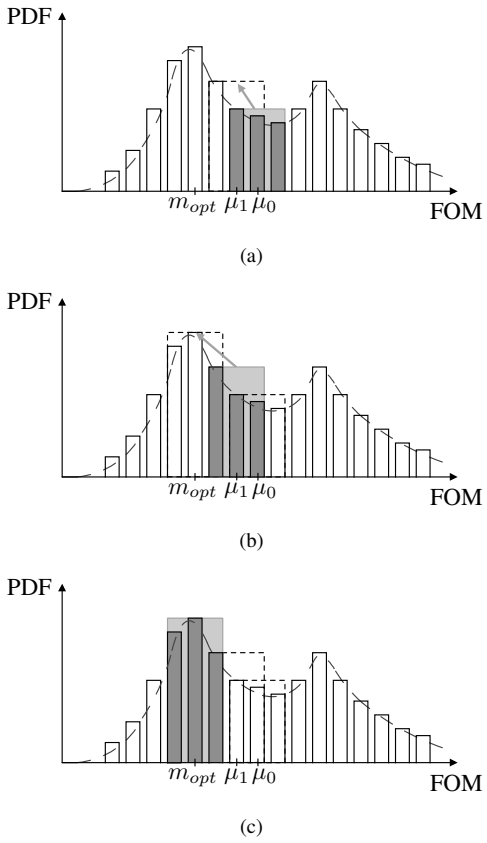


Fig. 3: Illustrative example for the matching algorithm (a) starting the selection from the global average μ_0; (b) selecting cells through local averages, μ_1; and, finally (c) determining a maximum of the PDF at m_{opt}.

the circuit cells of an integrated circuit. Although it may not represent the right initial designed specification (yet probably close), it certainly defines the largest group of similar cells. Hence, the goal is then to search for a maximum on a PDF that is not known a priori. A very simple algorithm is employed similar to gradient ascent, but with a reasonable simple digital implementation, which does not require standard A/D or D/A converters.

The iterative process starts at a given point of the PDF, μ_0 as seen in Fig. 3a, which is the initial condition resultant from the global average. An interval around this point defines the desired tolerance (shadowed regions in Fig. 3). This tolerance is kept fixed along all the iterative process. In a next step, a local average FOM is computed only for the cells that fall within this interval. The new average value moves up the PDF hill since the highest slope side of the local mean will have a stronger weight on the result, i.e. μ_1 shown in Fig. 3b. This process is repeated until the algorithm halts at a confined region. As long as the predefined tolerance allows for inclusion of different number of selected cells, the final result corresponds to a (local, or maybe global) maximum of the PDF, i.e. the mode m_{opt} as depicted in Fig. 3c.

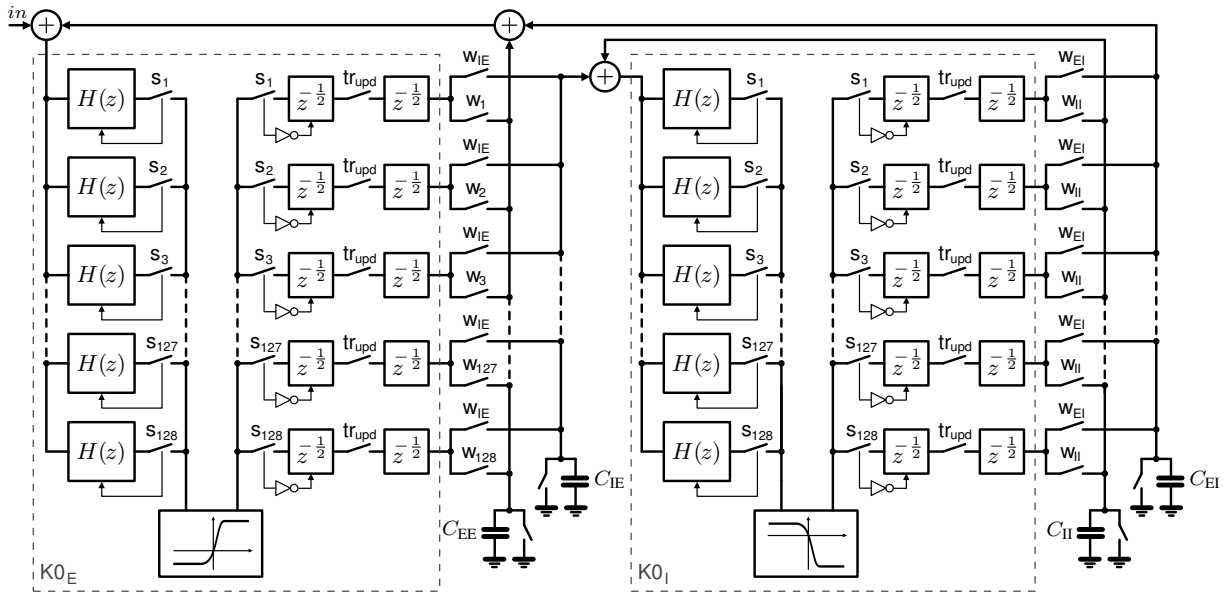


Fig. 4: Channel-multiplexing scheme for the RKII network.

III. System Implementation

The RKII network is formed by interconnecting a certain number of RKII cells between all the $K0_E$-$K0_I$ cell pairs. Rapidly, the number of interconnections become massive as the number of cells (channels) increase, actually in the order of $O(N^2)$. Hence, interconnectivity becomes a limiting factor in the network realization. However, if the connectivity matrix is multiplexed, then the order can be reduced to $O(N)$, moving the complexity control from analog into the digital domain [14]. Since many of the parameters are common to all cells, these can also be multiplexed (e.g. sigmoids, weighting capacitors), increasing the efficiency in the use of resources. Fig. 4 shows the multiplexing scheme adopted in this work. The system is analog but discrete in time. Actually, this approach benefits the BIST design because many of the resources can be readily reused for such purpose, while dramatically reducing the overhead of analog test hardware.

Both $K0_E$ and $K0_I$ cells present very similar structures, except for their static nonlinearities. Although the formal representation is the same, the relative outputs are mirrored along the input axis. This allows for the network weights to be all positive, which reduces the complexity of the weight multipliers to two quadrants. The same programmable non-symmetrical sigmoid circuit [15] has been used. Regarding the second-order dynamics, a discrete-time circuit based on the Filter-and-Hold (F&H) technique [16] is employed to obtain the relatively low-frequency poles at 35- and 114-Hz [17]. The memory cell z^{-1} plays an important role in the RKII multiplexing scheme, and in the proposed test method as well. This block is implemented using an SI delay with two second-generation class-A memories $z^{-1/2}$, improved by means of regulated-cascode circuits [18], [19]. As the current is held constant at reading clock-phases, the weighting operation can be accomplished by simply integrating constant currents through a capacitor during predefined time intervals. This also allows for multiplexing of the weighting block by reading each memory output current at different sample times. In fact, linear current-voltage conversion is achieved with simple digital control, which is suitable for our test purposes.

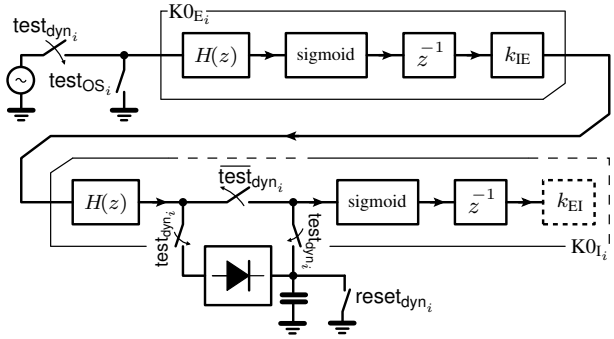


Fig. 5: Diagram for the test modes included in $K0_E$–$K0_I$ cells.

A. BIST design

The proposed approach allows two different tests to be performed at all rows of the network, each one consisting of a $K0_E$–$K0_I$ cell-pair as depicted in Fig. 5. First, since offsets can be a critical issue in the analog system operation, an initial attempt is performed to discard any cells affected by excessive offset levels. Secondly, considering solely the cells selected at the end of the offset test, new comparisons are applied based on cell dynamics. In both testing procedures the $K0_E$–$K0_I$ sets are treated independently. That is, only a $K0_E$ and its respective $K0_I$ cell are activated at a time, with feed-forward connections and no lateral connectivity.

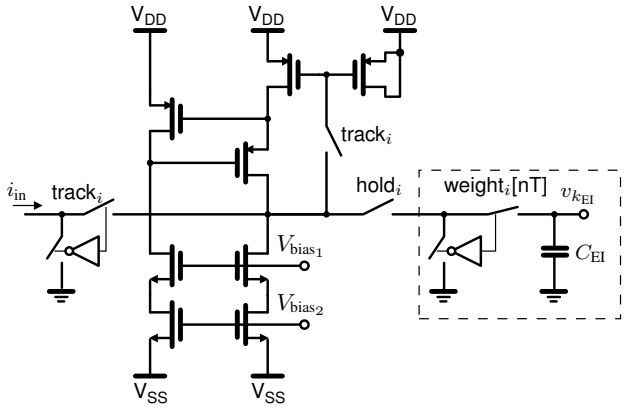


Fig. 6: SI memory $z^{-\frac{1}{2}}$ with weighting circuit applied.

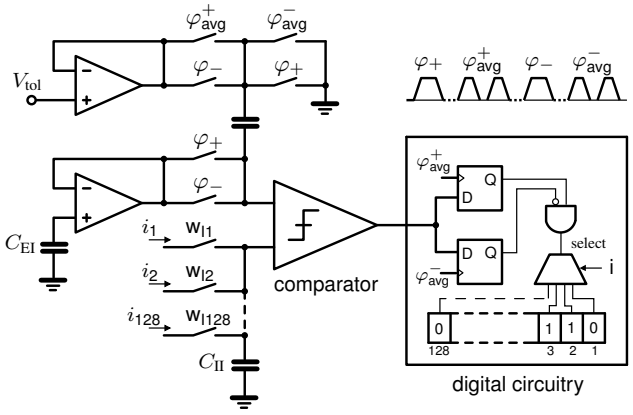


Fig. 7: Comparative references for selecting/deselecting cells.

During the offset test, the cell inputs are connected to ground. The clock sequences used in nominal operation are sufficient to hold the offset current at the last memory of the $K0_E$–$K0_I$ chain (memory of the $K0_I$). In the case of dynamics testing, steady-state magnitude response is used as comparative figure-of-merit. Experiments with impairments in cell parameters revealed unequal magnitude responses for each $K0_E$–$K0_I$ cell. Hence, the steady-state magnitude is adopted as signature for similarity. The test stimulus is a sinusoidal voltage applied at the cell inputs. A conventional voltage peak-detector [20] is employed at the output of the filter on the inhibitory side. The same detector is used in each test, repeated for each $K0_E$–$K0_I$ set. This way, any eventual systematic error is not observed as an actual mismatch because it affects all cells evenly. However, reduced amplitude is used to prevent saturation by the nonlinearities, which would mask the F&H magnitudes. Furthermore, the turn-on time instant for the peak-detector is delayed a few clock cycles in order to capture the steady-state signal, avoiding the transient behavior.

The computation for the average in offset and dynamics tests, as required by the proposed test methodology, is essentially based on the same procedure. Once the SI memories hold the offset or peak values (Fig. 6), the weighting-capacitor multiplier is used to obtain the corresponding average. The number of selected cells must be taken into account for this procedure, so that the weight value is computed accordingly. This scaling is partly done in the digital domain. The number 1280 (128 cells $\times$ 10 clock-cycles) is divided by the number of selected cells, to define a time interval. This corresponds to the time slot that any given cell (among those selected) must be connected to the capacitance C_{EI} to compute a new average value. Since the result can be a non-integer value, the resulting accuracy achieved in this operation depends on the number of clock-cycles considered. The weighting circuit runs all selected cells, integrating the currents that are held in each SI memory during the time slot previously determined. At the end, the capacitance C_{EI} stores the corresponding average value for an iteration. New sets of cells must be now determined based on the resulting average. A voltage

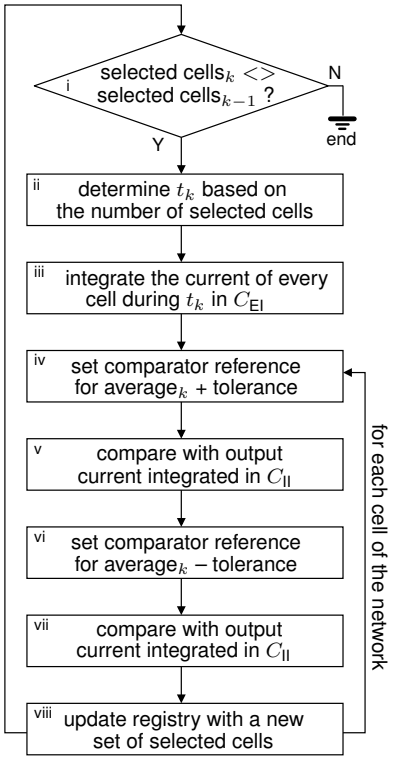
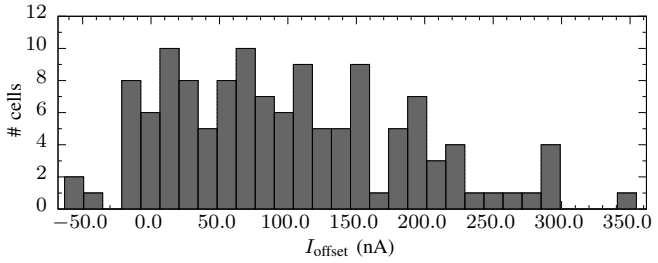
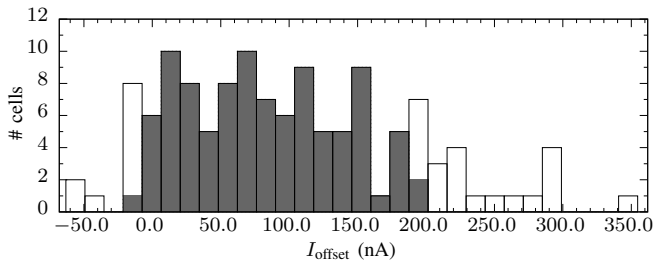


Fig. 8: Flowchart for the selection/deselection algorithm implementation.

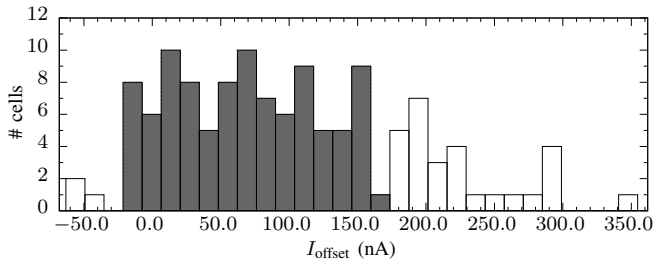
comparator has been designed based on [21], which is used with a predefined tolerance value as reference. This takes place in two steps in which lower and upper bounds are evaluated separately, so that the same comparator can be employed. Fig. 7 shows the proposed approach to address the cells from the network (whether or not selected) and determine if the peak/offset is within the expected limits. The iterative procedure regarding selection of cells is summarized in Fig. 8. Whenever a cell is tested, its output current needs to be integrated again. However, C_{II} is now used to avoid loosing the average stored in C_{EI}.



(a)

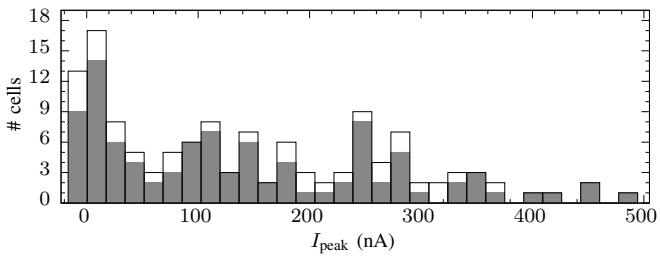


(b)

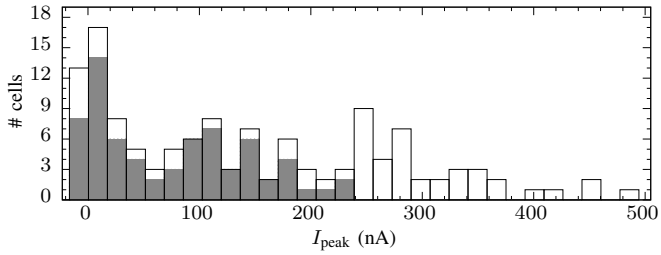


(c)

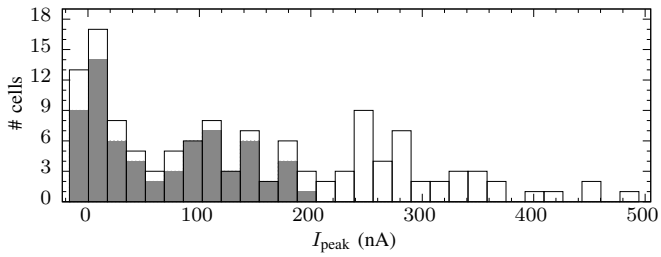
Fig. 9: Offset test results, from the (a) first iteration; through (b) second iteration; to (c) sixth iteration as the final result.



(a)



(b)



(c)

Fig. 10: Dynamics test results with (a) first selection; (b) third iteration; and (c) final result at the sixth iteration.

IV. Results

A network comprised of 128 channels is designed to validate our test approach. The network and mixed-signal test circuits are designed using a 180-nm CMOS process, with 1.8-V power-supply, comprising BSIM3v3 charge-conservative models. Monte-Carlo simulations are performed at one cell to obtain the statistical description of process variations and parameter mismatches in the entire set of cells. This is also applied to circuitry included for testing purposes. The circuits are simulated using Virtuoso AMS Designer simulator from Cadence. The digital test control has been implemented at RTL level.

Fig. 9 shows the results for the offset test, which is the first to be performed. The shadowed regions denote amounts of selected cells. As early referred, these currents correspond to those in Fig. 7, which are scaled into voltages by integration. The digital circuitry operates at the rate of 32-MHz, to obtain an integration time window of 80-μs. Among the 128 cells, 97 cells have been chosen presenting the most similar offset characteristics. From this pull of cells, the next step in the proposed methodology is to find the ones with identical dynamics. As shown in Fig. 10, a final set of 67 cells is selected. The complete algorithm takes solely 12 iterations, 6 iterations in each test.

The comparator resolution has a great impact on the final result for both tests. That is, it imposes the tolerance limits, and has strong impact in the stop criteria as well. For the offset test, 80-mV is chosen as tolerance value, while dynamics uses 100-mV. These values were defined based on the typical operating conditions for this particular system, including the resolution and offset of the comparator (around 15-mV). Hence, the value for the integration time has been determined to minimize these effects. The same algorithm has been applied with Matlab validating the proposed approach.

The proposed test method can be applied in offline mode at the circuit setup to compensate for aging effects and similar variations on the circuits. Moreover, since the selected cell-array is stored digitally, it can be easily applied for diagnose purposes.

V. Conclusion

In this paper we have proposed a methodology and its mixed-signal realization for matching detection of circuit cells in RKII networks. A 128-cell reduced-KII network has been designed in a standard 180-nm CMOS technology. The test method has been validated through Monte-Carlo simulation to obtain process variations and mismatches between the cell circuits. The dc offset as well as the dynamic performance of several cells were used as comparative terms to detect a set of cells that most resemble in these characteristics. This is accomplished within tolerance levels that can be easily programmed for both tests. The cells within tolerable performance are chosen to reconfigure the network, while turning off cells with less-tolerable mismatches.

Most of the network building-blocks are used to perform the RKII self-test, namely the SI current-memories and multiplier weighting circuits. With little overhead on digital circuitry, the proposed test approach can be further extended to other networks comprising repeated structures, such as typical artificial neural networks.

Acknowledgment

This work is funded by the ERDF through the Programme COMPETE and by the Portuguese Government through FCT - Foundation for Science and Technology, project ref. CMU-PT/SIA/0005/2009, and also by FCT Grant BD/28163/2006. The authors would like also to thank Daniel Oliveira from the Microelectronics' Students Group at FEUP for the help provided in Monte-Carlo distributed simulations, and process design-kit configurations.

References

[1] S. Geman, E. Bienenstock, and R. Doursat, "Neural networks and the bias/variance dilemma," *Neural Computation*, vol. 81, pp. 1–58, Jan 1992.

[2] F. Warkowski, J. Leenstra, J. Nijhuis, and L. Spaanenburg, "Issues in the test of artificial neural networks," in *Proceedings of the IEEE International Conference on Computer Design: VLSI in Computers and Processors*, Oct 1989, pp. 487–490.

[3] G. E. Sæther, C. Toumazou, G. Taylor, K. Eckersall, and I. M. Bell, "Built-in self test of S^2I switched current circuits," *Analog Integrated Circuits Signal Processing*, vol. 9, pp. 25–30, Jan 1996.

[4] J.-S. Wang, W.-H. Huang, and C.-L. Wey, "Fault simulation of built-in tester for CMOS switched-current circuits," in *Proceedings of the 1998 Midwest Symposium on Systems and Circuits*, Aug 1998, pp. 212–215.

[5] Y. Lechuga, R. Mozuelos, M. Allende, M. Martnez, and S. Bracho, "Fault detection in switched current circuits using built-in transient current sensors," *Journal of Electronic Testing*, vol. 21, pp. 583–598, 2005.

[6] A. Laknaur and H. Wang, "Built-in-self-testing techniques for programmable capacitor arrays," in *Proceedings of the 6th International Symposium on Quality Electronic Design*, Mar 2005, pp. 434–439.

[7] J. Velasco-Medina, I. Rayane, and M. Nicolaidis, "AC/DC BIST for testing analog circuits," in *Proceedings of th 12th Annual IEEE International ASIC/SOC Conference*, 1999, pp. 223–227.

[8] W. J. Freeman, *Mass Action in the Nervous System*. New York, NY: Academic Press, 1975.

[9] J. Príncipe, V. Tavares, J. Harris, and W. Freeman, "Design and implementation of a biologically realistic olfactory cortex in analog VLSI," *Proceedings of the IEEE*, vol. 89, no. 7, pp. 1030–1051, Jul 2001.

[10] W. Freeman, "Tutorial on neurobiology from single neurons to brain chaos," *International Journal of Bifurcation and Chaos*, vol. 2, no. 3, pp. 451–482, Sep 1992.

[11] J. J. Hopefield, "Neurons with graded response have collective computational properties like those of two-state neurons," *Proc. Natl. Acad. Sci. USA*, vol. 4, pp. 3088–3092, Feb 1984.

[12] S. Biswas, P. Li, R. D. Shawn Blanton, and L. T. Pileggi, "Specification test compaction for analog circuits and MEMS," in *Proceedings of the Design, Automation and Test in Europe Conference and Exhibition*, vol. 1, Mar 2005, pp. 164–169.

[13] B. Varaprasad, L. M. Patnaik, H. S. Jamadagni, and V. K. Agrawal, "A new ATPG technique (ExpoTan) for testing analog circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 26, no. 1, pp. 189–196, Jan 2007.

[14] V. G. Tavares, S. Tabarce, J. C. Príncipe, and P. G. Oliveira, "Freeman olfactory cortex model: A multiplexed KII network implementation," *Journal of Analog Integrated Circuits and Signal Processing*, vol. 50, no. 3, pp. 251–259, Mar 2007.

[15] S. Tabarce, V. G. Tavares, and P. G. Oliveira, "Programmable analogue VLSI implementation for asymmetric sigmoid neural activation function and its derivative," *Electronics Letters*, vol. 41, no. 15, pp. 863–864, Jul 2005.

[16] V. G. Tavares, J. C. Príncipe, and J. Harris, "F&H filter: A novel ultra low power discrete time filter," *Electronics Letters*, vol. 35, no. 15, pp. 1226–1227, Jul 1999.

[17] J. Príncipe and V. Tavares, "Design and implementation of biologically realistic signal to symbol translators," in *Proceedings of the 23rd Annual International Conference of the IEEE Engineering in Medicine and Biology Society*, vol. 4, 2001, pp. 4096–4099.

[18] E. Sackinger and W. Guggenbuhl, "A high-swing, high-impedance MOS cascode circuit," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 1, pp. 289–298, Feb 1990.

[19] C. Toumazou, J. Hughes, and D. Pattullo, "Regulated cascode switched-current memory cell," *Electronics Letters*, vol. 26, no. 5, pp. 303–305, Mar 1990.

[20] H.-C. Chow and I.-H. Wang, "High performance automatic gain control circuit using a S/H peak-detector for ASK receiver," in *9th International Conference on Electronics, Circuits and Systems*, vol. 2, 2002, pp. 429–432.

[21] M. Bazes, "Two novel fully complementary self-biased CMOS differential amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 26, no. 2, pp. 165–168, Feb 1991.