Signal Integrity and Interconnections Test on Technical Fabrics

Andreina Zambrano
INESC TEC (former INESC Porto), Rua Dr. Roberto Frias, 378, 4200-465 Porto, Portugal
andreina.c.zambrano@inescporto.pt

José Machado da Silva
INESC TEC (former INESC Porto), Faculdade de Engenharia, Universidade do Porto, Rua Dr. Roberto Frias, 4200-465 Porto, Portugal
jms@fe.up.pt

Abstract — **The use of textile yarns as data transmission media enables the design of non-obtrusive well-fitting garments as wearable systems. However, textile conductive yarns show impedances higher than those presented by common metal conductors and these values can change with the textile condition and level of stretching, affecting the integrity of the transmitted signal. This work proposes a built-in self-test methodology to test textile yarn interconnections for conventional stuck-at, open and short faults, as well as to verify signal integrity. The test procedure being proposed relies on sampling to generate a digital signal that results from comparing the received signal with pre-defined voltage levels. The obtained signature allows to verify signal integrity parameters: V_{Lmax}, V_{Hmin} and rise and fall times. Simulation results confirm the validity of the methodology being proposed.**

Keywords-; Signal integrity; Technical textile; Built-in self-test

I. INTRODUCTION

During the last decade, smart textiles have received an increasing attention as a research domain due to the growing interest on their applications in different fields, such as medicine, sport, and entertainment. The merge of textile and electronic technologies enables the design and production of wearable well-fitting garments provided with non-obtrusive distributed sensors and electrodes [1].

The combination of functional clothes, integrated electronics and on-body processing, is defined as an e-textile system, where electronics are incorporated into fabric by means of woven, knit, or as a composite. An e-textile system differs from conventional electronic systems, in that electrical and physical features operate symbiotically and can affect the functionality and properties of each other [2].

The presence of common electrical (cupper) wires makes wearable systems not comfortable. Research has been made to develop textile conductors that show conductivity characteristics similar to electrical conductors, while being flexible as textiles. Different conductive yarns have been developed with this purpose. These offer advantages compared to normal metal conducting wires as they can be integrated unobtrusively into clothing and are comfortable to wear. Nevertheless, those currently available are limited in electric conductivity and, more importantly, do not show stable impedance characteristics.

In e-textile systems, conductive yarns can be used as a transmission medium to exchange data between system nodes as well as for powering purposes [3]. However, as the wearer changes his/her body posture, the line impedances vary. Also, as the garment is successively washed, the conductors progressively deteriorate [1] [4] Consequently, these variations could lead to signal integrity problems, that is, signals tend to show inadequate amplitude and timing characteristics [5].

Signal integrity has become a concern in different electronic systems, as cross-coupling, mutual inductance and capacitive effects among wires of a link, affects signals' information due to added noise and delay. These are also responsible for performance degradation, shorter life time and reliability concerns. That is the case also, namely, within Network on Chip (NOC) cases, where the use of nanometer technology magnifies various parasitic factors which are difficult to control during fabrication [6] [7].

The work presented herein addresses the issue of testing interconnections made with textile conductive yarns, in order to ensure reliable data transmission on this type of medium. The boundary-scan test methodology was initially introduced to facilitate interconnect testing among integrated circuits on a board, for stuck-at, open and short faults. However, textile yarns besides open and short faults, can also experiment signal degradation issues due to variable impedance values, raising consequently the issue of performing tests to check signal integrity [8].

The textile yarn interconnections test methodology being proposed aims, besides detecting conventional stuck-at, open and short faults, verifying also signal integrity issues, caused by yarns' variable electrical characteristics. This verification is performed basically by checking whether the received signal amplitude and timing fit pre-defined acceptable margins, even when affected by amplitude noise and delay.

The presence of these perturbations in data communication can cause intermittent logic-errors. These are very difficult to test and debug due to their unpredictable nature (e.g. depending on data, parasitic values, interaction, environment, etc.). Although it is impossible and often unnecessary to eliminate all noise sources, signal integrity must be verified to assure correct system functionality [9] .

The remainder of this paper is organized as follows. Section II discusses signal integrity issues, section III presents the test methodology being proposed and simulated test cell, Section IV reports preliminary simulation results which illustrate and

confirm the validity of the methodology being proposed. Section V highlights the main conclusions and future developments of this work.

II. Signal Integrity

A signal with good integrity characteristics is defined as one which when observed at the receiver end occurs within the desired time window and with adequate amplitude levels. Signal integrity problems can be caused by interconnects degradation or by external interference. Figure 1 illustrates different manifestations of signal integrity degradation [10] [11]:

- a high logic voltage level lower than the minimum high acceptable level,
- a low logic voltage level higher than the maximum acceptable low level
- excessive signal delay - a rising/falling edge shows skews longer than the acceptable timing windows
- overshoot, undershoot and glitch
- ringing and oscillation
- long settling time.

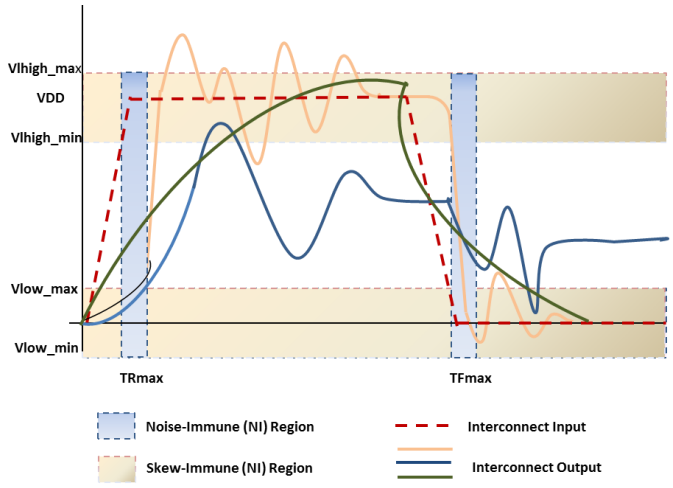

Figure 1.Signal integrity hazards.

These effects are aggravated with raising frequency or increasing conductors' impedance characteristics. The conductors' impedance RLC values depend on many factors including the operating frequency and the length of the interconnection [3]. Textile yarns show impedance values higher than common metal conductors and these values can change with the textile condition and level of stretch, affecting the characteristics of the transmitted signal.

Researchers as Didier Cottet [12] treated textile yarns as line transmission media to know their electrical characteristics, by means of Time Domain Reflectometry (TDR). A vector network analyzer (VAC) can be used in case it is necessary to know the impedance value at different frequencies.

Previously to the design of the proposed test methodology, the electrical characterization of different yarns was performed. Table 1 shows impedance values at 10 MHz of two textile yarns in relaxed and stretched states. It can be observed that textile conductive yarns show a resistive and inductive impedance behavior, which decrease as the yarn is stretched and are frequency dependent i. e., $\boldsymbol{Z}(\mathrm{f}) = r(\mathrm{f}) + j2\pi\omega l(\mathrm{f})$.

The Smith chart in figure 2, shows the impedance variation with frequency of one spun yarn made with a mixture of a non-natural fiber, like polyester, and stainless steel fibers (60 cm long), in the range 9 kHz to 10 MHz. The conductive yarn interconnection has then been modeled as a series R-L impedance whose values were obtained from a laboratory characterization of several textile yarns. Additionally, one capacitor is placed at each end of the interconnection to model capacitive coupling effects as well as circuits' output and input capacitances.

TABLE I. Yarns' Electrical Characteristics

Yarn	Relaxed (natural length)		Stretched (1.5 natural length)	
	Ω /cm	nH/cm	Ω /cm	nH/cm
1	0.65	16.4	0.47	6.68
2	6.76	35	4.43	33

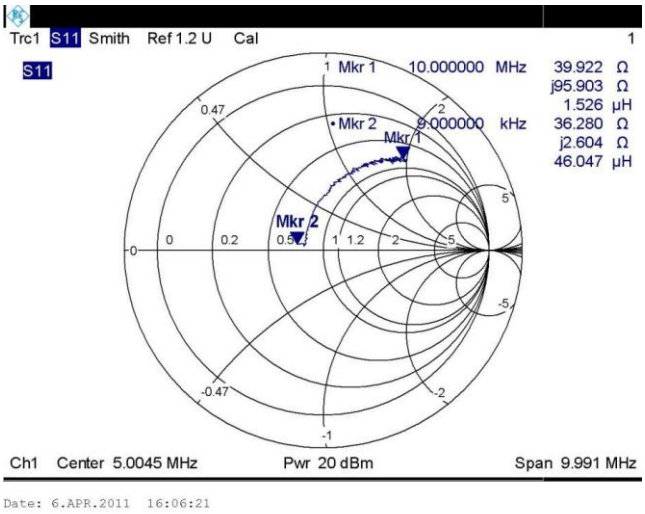

Figure 2. Impedance Smith chart of a textile conductive yarn.

Considering the higher impedance of data transmission lines made of textile conductive yarns, the first consequence is a bandwidth limitation. Then, one has to take into account the impedance variation. Although the simple consideration of the worst case impedance would allow determining the maximum safe bit rate that could be used, this in fact is not as immediate as that, once other external factors, such as aging and particles contamination, may affect that impedance. It is then likely that with the use of textile conductive yarns for data communication, the signals suffer different perturbations leading to data integrity issues.

As far as logic circuits (namely the CMOS ones) are concerned, 1 and 0 logic levels are recognized if the respective

voltage values occur in the, respectively, [V_{IH},V_{DD}] and [V_{SS}, V_{IL}] acceptable noise margins, being VIH and VIL respectively, the minimum accepted voltage for a 1 logic value and the maximum voltage permitted for a 0 logic value. Likely, tolerance margins can also be defined concerning timing, that is, regions of acceptance of a certain delay for rising and falling times.

In practice, having noise-immune (NI) and skew-immune (SI) regions been defined, any portion of signal occurring outside NI and SI regions signals leads to an integrity loss issue [13]. The size of these regions depends of the manufacturing technology being used.

III. TEST METHODOLOGY

The IEEE 1149.1 boundary-scan test standard has been widely accepted in the test community. The standard provides convenient and not complex testing features, to detect open and short interconnect faults. The IEEE 1149.4 mixed-signal test bus standard was proposed to allow accessing analog pins of a mixed-signal device. In addition to the ability to test interconnections using digital patterns, 1149.4 includes the ability to measure actual passive components, such as resistors and capacitors. The IEEE 1149.6 standard provides a solution for testing AC-coupled interconnections between integrated circuits on printed circuit boards and systems [6].

The standards mentioned above, provide means for testing the core logic and the interconnections among integrated circuits. However, interconnections can be tested for stuck-at, open and short faults, but not for signal integrity

The test methodology being proposed here aims to test interconnects also for hazards that yield integrity loss. The objective is to ensure that data can be correctly identified by the receiving node. The test procedure is based on generating a digital signature with 0/1 values corresponding to the received signal crossing specific pre-defined threshold voltage levels within expected time intervals, as it is show in figure 3.

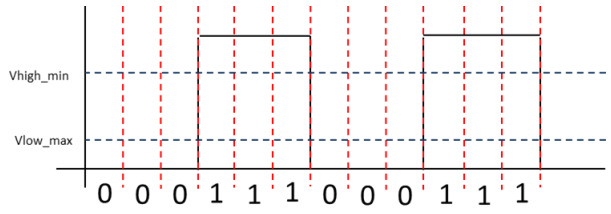

Figure 3. Digital characterization of signal integrity.

The digital signature captured from the test operation is obtained using sampling, a technique usually employed for measuring timing specifications in digital applications. This technique is based on sampling the signal with a high time resolution and performing time domain analysis by the set of threshold crossings to estimate timing specifications [14]. In this work threshold crossings correspond to V_{IL} and V_{IH}.

The sampling frequency defines the number of samples per unit of time taken of the test signal. The value of the sampling period should be adequate to detect correct bit changes at each transition time and should be related with the maximum allowed rise/fall time at the receiving node. If the sampling period is much shorter than the maximum allowed rise/fall time, a high time resolution is obtained but also a higher number of redundant bits are captured (figure 4a). In case the sampling period is longer than the maximum permitted rise time (figure 4b), even if the received signal experiences a transition time longer than allowed, a correct bit change can be generated at each sampling time, hiding then transition time faults.

A good compromise to define a proper sampling period to generate a correct bit sequence is making it approximately equal to the maximum permitted rise time (figure 4c).

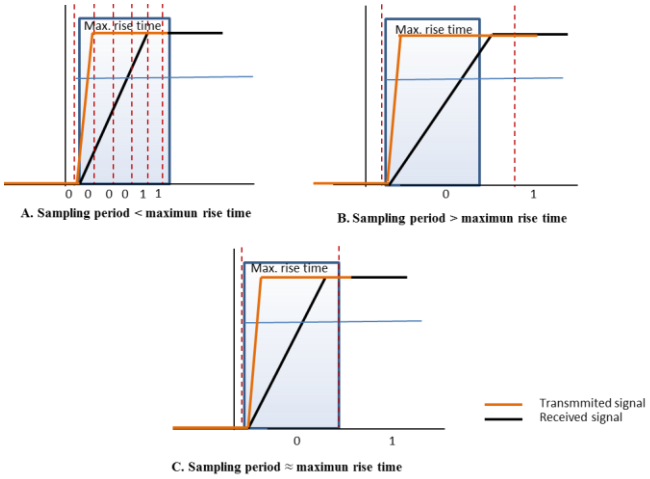

Figure 4.Sampling frequency *vs*. Maximum rise time.

The rise time parameter is related with the characteristics of the system in transient regimen. A RLC system such as the yarn interconnection can be approximated to a second-order system that is characterized by (1) [15]

$$\frac{\partial Vout(t)^2}{\partial t^2} + 2\zeta\omega_n \frac{\partial Vout}{\partial t} + {\omega_n}^2 Vout = Vin(t) \quad (1)$$

$$\zeta = \frac{R}{2} \times \sqrt{\frac{C}{L}} \qquad \omega_n = \frac{1}{\sqrt{LC}} \quad (2)$$

where R and L are the resistance and inductance of the conductive yarn and C is the total capacitance for coupling effect.

The second order system performance, can be characterized by the parameters: peak time, settling time, rise time and maximum overshoot. The rise time for an under-damped system, with $0.3 < \zeta < 0.8$, can be calculated with (3):

$$t_R \cong \frac{2.16\zeta + 0.6}{\omega_n} \quad (3)$$

Equation 3 gives an estimate of the rise time obtained for a RLC model of the yarn interconnection. If the input signal rise time is also considered, the total rise time at the receiver node is calculated with (4).

$$t_R\ total = \sqrt{{t_{Rinputsignal}}^2 + {t_{Rinterconnection}}^2} \quad (4)$$

If $t_{inputsignal} \ll t_{interconnection}$

$$t_R total \cong t_{Rinterconnection}$$

From the rise time given with the nominal impedance of the yarn interconnection, the maximum allowed rise time can be defined. The test stimuli sequence should present a frequency lower than the adopted sampling frequency and usually is the frequency of normal operation.

The digital sequence obtained after sampling, is then compressed by means of a Multiple Input Signature Register (MISR) and compared with the expected golden signature.

Figure 5, illustrates this detection process. Signal A represents a perfect digital signal with bit changes occurring at the proper transition times, indicating good rise and fall times. Signal B shows noise at low and high voltage values, yielding a digital representation different from that obtained with the golden signal A. The presence of noise in the high value leads bit 4 of V_{Hmin} output changing to 0 instead of maintaining a 1; noise in the 0 logic value, makes that the V_{Lmax} output shows a 1 instead of a 0. Due to the long fall time, signal B does not show a change in bit 5,6 as in signal A. Although the rise time of the first pulse is longer than that in signal A, its value does not exceed the maximum acceptable rise time and then correct bit changes are obtained in time slices 2, 3 and 4.

It can be observed in signal B that any of signal integrity violations on V_{Lmax}, V_{Hmin}, fall time or rise time, generates a change in the bit sequence obtained after sampling and in the signature generated with the MISR. Therefore when this code is compared with the golden code, a problem in the interconnection is detected.

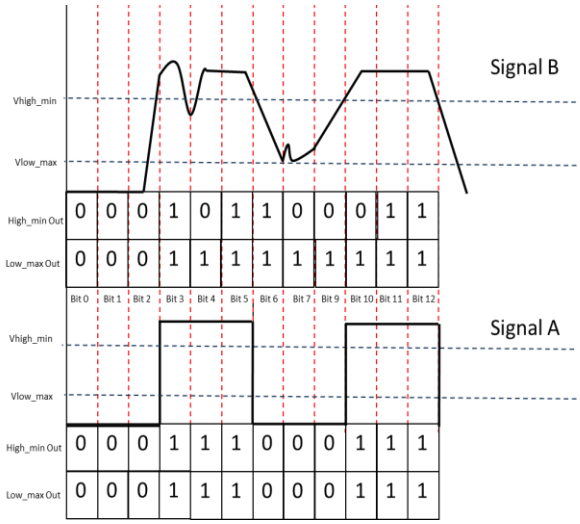

Figure 5. Signal integrity violations.

BIST techniques can be classified in two categories, namely on-line, when testing is performed during normal functional operational conditions, and off-line BIST, when the circuit under test is stimulated with a specifically designed test pattern and eventually configured in a different operating mode [16]. In this case, as the objective is to carry-out on-line testing, it is then necessary to capture test signatures at transmitter and receiver sides, which are after compared for analysis purposes. In the case of off-line testing, it is possible to preload the golden test signature at the receiver side to compare it with the signature obtained with the MISR.

A. *Simulated test cell*

Figure 6 shows a simple schematic of the circuitry required to implement the testing methodology being proposed. Besides the PRBS generator placed in the emitter end of the interconnection, one can see also signal evaluators and signature compression (SESC) circuits in both ends. As previously stated, in the on-line mode normal operation signals are used as test patterns and both SESC circuits are needed to obtain the expected and the actually obtained signatures. In the off-line mode a PRBS generator is used and only the SESC circuit placed in the receiving end is needed.

The comparison between golden and the actually obtained signatures involves the use of a communication protocol, whose details are not subject of this paper.

The off-line mode was simulated using one PRBS generator in the emitter side generating a sequence of 32 bits at 10 MHz, which is the mission operating frequency to be used within these interconnections, defined after the typical expected yarn impedances.

The received waveform is compared with the specified V_{ILmax} (30% of VDD) and V_{IHmin} (70% of VDD) values with comparators clocked at a sampling frequency of 50 MHz. The MISR generates a 5-bit signature that is transmitted back to the emitter for comparison with the expected golden signature. Notice that in a mesh network scenario alternative paths are available to send information between nodes.

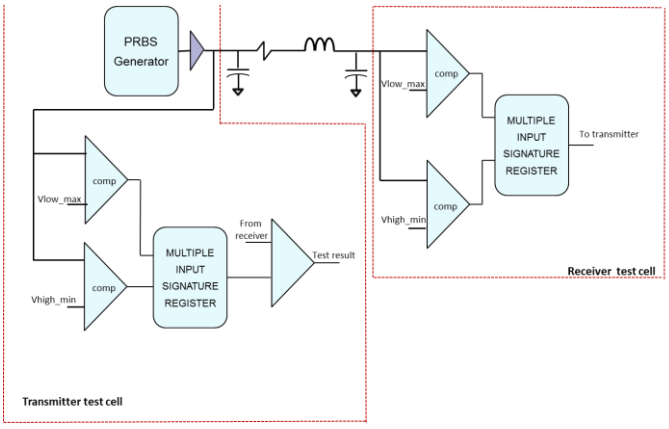

Figure 6. Simulated test cells.

IV. RESULTS

The initial values of the RLC model, shown in figure 6, were taken as the golden ones and were then increased up to by

100% to check if the proposed test methodology allows detecting signal integrity violations. Table II shows the signatures obtained at the receiver side for different impedance variations.

With an increment up to 30% of inductance and resistance values, the signature obtained at the receiver side is correct. For an increase of 40%, a violation of the rise time parameter occurs and the test signature is different from the golden code.

Between 50% and 100%one can observe the same incorrect codes in all cases, because the occurring signal integrity issues are always caused by longer rise and fall times.

A different incorrect signature was obtained when resistance and inductance values were separately increased 10 times. In both cases the received signal experienced a violation of the 4 signal integrity parameters studied. As the signal shows different behaviors in each of these two cases, different incorrect codes are obtained.

TABLE II. TEST SIGNATURES (GOLDEN: 00000)

Impedance variation	Receiver MISR
0%	00000
10%	00000
20%	00000
30%	00000
40%	00100
50%	11101
60%	11101
70%	11101
80%	11101
90%	11101
100%	11101
1000% - R	10101
1000% - I	11110

Figure 7 shows the received signals obtained with different impedance values. The first signal shows the stimulus test sequence. The second signal shows the signal received in the case of nominal impedance. The third signal shows the received signal with a 50% increase of the resistance and impedance values of the RLC interconnection model. It can be observed that the voltage value satisfies the requirements but fall and rise times are 30% longer, approximately.

V. CONCLUSIONS AND FUTURE WORK

Signal integrity is degraded in data communications as signals propagate through interconnections. An integrity loss may lead to functional errors, especially in a transmission medium such as textile conductive yarns, which show variable impedance characteristics. This work addresses this issue and proposes a built-in self-test methodology to test textile yarn interconnections by checking whether a received signal amplitude and timing fit pre-defined acceptable margins. Preliminary simulation results show that with this methodology it is possible to define tolerance bands after proper selection of upper and lower threshold voltages and sampling frequency. All the faulty interconnection impedances simulated could be correctly detected as generating signal integrity hazards.

Future work will look for the possibility of performing diagnosis after the analysis of the obtained faulty signatures. The purpose is not just detecting a bad medium transmission, but also to identify the textile yarns condition , before they become useless for correct data transmission.

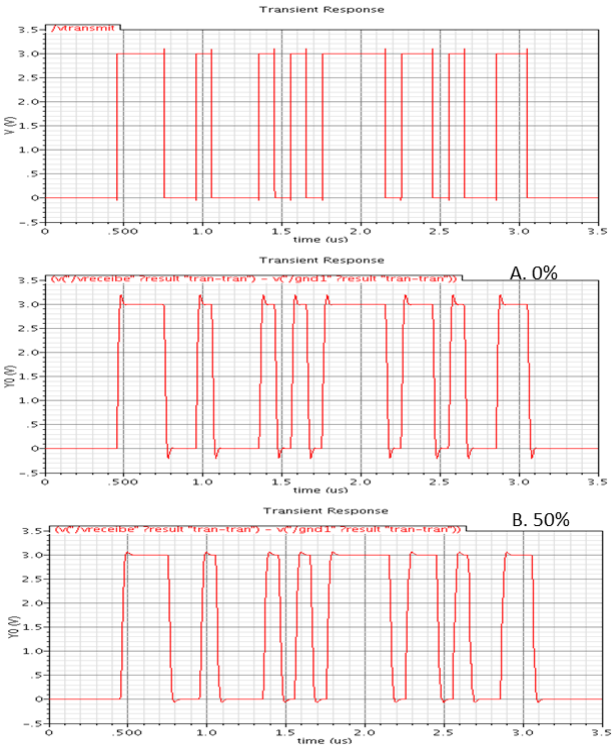

Figure 7. Test bit sequence.

ACKNOWLEDGMENTS

This work has been funded by the ERDF - European Regional Development Fund - through the COMPETE Programme (operational programme for competitiveness), by National Funds through FCT – Fundação para a Ciência e a Tecnologia (Portuguese Foundation for Science and Technology) - within project PTDC/EEA-ELC/103683/ 2008 and contributed to project Eureka/Catrene TOETS CT302.

REFERENCES

[1] T. Kirstein, D. Cottet and J. a. T. Grzyb, "Textiles for Signal Transmission in Wearables," in *Proceedings Workshop on Modeling, Analysis and Middleware Support for Electronic Textiles*, San Jose, California, 2002.

[2] L. Beckmann, C. Neuhaus, G. Medrano, N. Jungbecker, M. Walter and T. a. L. Gries, "Characterization of Textile Electrodes and Conductors Using Standardized Measurement Setups," *Physiological measurement*, vol. 31, no. 2, pp. 233-247, 2010.

[3] E. Wade and H. Asada, "Wearable DC Powerline Communication Network Using Conductive Fabrics," in *IEEE International Conf. Robotics and Automation (ICRA 04)*, 2004.

[4] L. Rattfält, M. Lindén, P. Hult, L. Berglin and P. Ask, "Electrical Characteristics of Conductive Yarns and Textile Electrodes for Medical Applications," *Medical and Biological Engineering and Computing*, vol. 45, no. 12, pp. 1251-1257, 2007.

[5] M. Nourani and A. Attarha, "Built-in Self-test for Signal Integrity," in *Design Automation Conference*, 2001.

[6] M. Nourani and A. Attarha, "Detecting Signal-overshoots for Reliability Analysis in High-speed System-on-chips," *Reliability, IEEE Transactions on*, vol. 51, no. 4, pp. 494-504, 2002.

[7] R. Nourmandi-Pour, N. Mousavian and A. Khadem-Zadeh, "BIST for Network on Chip Communication Infrastructure Based on Combination of Extended IEEE 1149.1 and IEEE 1500 Standards," *Microelectronics Journal*, vol. 42, no. 5, pp. 667-680, 2011.

[8] R. Nourmandi-Pour and A. a. M. R. A. Khadem-Zadeh, "An IEEE 1149.1-based BIST Method for At-speed Testing of Inter-switch Links in Network on Chip," *Microelectronic Journal*, vol. 41, no. 7, pp. 417-429, 2010.

[9] A. Attarha and M. Nourani, "Testing Interconnects for Noise and Skew in Gigahertz SoCs," in *Test Conference*, 2001.

[10] J. Liu, W. Jone and S. Das, "Pseudo-Exhaustive Built-in Self-Testing of Signal Integrity for High-Speed SoC Interconnects," in *Instrumentation and Measurement Technology Conference Proceedings, IEEE IMTC 2007*.

[11] N. Hernandez and V. Champac, "Testing Skew and Logic Faults in SoC Interconnects," in *Symposium on VLSI, 2008. ISVLSI '08. IEEE Computer Society Annual*, 2008.

[12] D. Cottet, J. Grzyb, T. Kirstein and G. Troster, "Electrical Characterization of Textile Transmission Lines," *IEEE transactions on advance packaging*, vol. 26, no. 2, pp. 182-190, 2003.

[13] M. Tehranipour, N. Ahmed and M. Nourani, "Testing SoC Interconnects for Signal Integrity Using Boundary Scan," in *VLSI Test Symposium, 2003*, 2003.

[14] S. Tabatabaei and A. Ivanov, "An Embedded Core for Sub-picosecond Timing Measurements," in *International test conference*, 2002.

[15] S. Kim and W. S, "Close-form RC and RLC Delay Models Considering Input Rise Time," *IEEE Transactions on circuit and systems*, vol. 54, no. 9, pp. 2001-2010, 2007.

[16] M. Abramovici, M. Breuer and A. Friedman, Digital Systems Testing and Testable Design, 1990.