

Basic Analog Circuits with a-GIZO Thin-Film Transistors: Modeling and Simulation

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Abstract—This paper addresses a modeling and simulation methodology for analog circuit design with amorphous-GIZO thin-film transistors (TFTs). To reach an effective circuit design flow, with commercially available tools, a TFT model has been first developed with an artificial neural network (ANN). Multilayer perceptron with backpropagation algorithm has been adopted to model the static behavior of the TFT devices, for different aspect ratios. The model was then implemented in Verilog-A, to allow a quick instantiation in circuit. Simulations using Cadence Spectre are performed to validate the model. On a second phase, simulation results of basic analog circuits, with this ANN model, are verified against the actual functional results, namely an adder, subtractor, and current mirror circuit. Results demonstrate not only the ANN model accuracy and compatibility with dc and transient analysis, but also show the a-GIZO TFT capability to perform analog operations.

I. INTRODUCTION

Transparent oxide conductors and semiconductors are key materials for a new generation of electronic devices, such as solar cells [1], transparent thin-film transistors (TFTs) [2] and even paper electronics employing the CMOS technology [3]. Particularly, amorphous gallium-indium-zinc-oxide (a-GIZO) TFTs are becoming interesting active elements for the design of electronic circuits. However, to achieve an effective design flow, accurate device models are required for computer-aided design (CAD) tools, to predict the small and large-signal behavior of the devices under simulation. TFTs with a-GIZO active layer are still much in the research field. Although rapidly evolving, no commercial models are yet available. A few papers have reported the development of physical models for a-GIZO TFTs [4], [5]. But many physical properties of the device, such as short channel and narrow width effects, still need to be properly characterized and modeled [6]. Moreover, physical models are complex and time consuming to realize. A modeling method, which is simple, accurate, continuous and with a less development time, is desirable for quicker electronic circuit design. As artificial neural networks (ANNs) show all the properties mentioned above, they are an excellent alternative to physical modeling for the current a-GIZO TFTs. Actually, ANNs have already been successfully applied to MOSFET modeling in the past [7]. In this work, multilayer perceptron (MLP) with backpropagation algorithm

is employed to model the static behavior of the TFT device. The MLP network is first trained with measured data. Once the network meets the performance goal, the MLP-ANN is implemented in Verilog-A, for standard use in circuit simulations.

There are several challenges involved in circuit designs with a-GIZO TFTs. Unlike the well-known CMOS technology, stable p-type transistors are not available and the devices exhibit threshold shifts due to bias stress [8]. Hence, circuit design is limited to the n-type a-GIZO TFTs. So far, designs with such devices have been confined to driving circuits [9], [10] and ring oscillators [11], [12]. The present paper characterizes the low-frequency behavior (ignoring parasitic capacitances) of basic building blocks in analog circuits with n-type enhancement a-GIZO TFTs. A subtractor and adder circuits from [13] are used as testbed, as well as a basic current-mirror.

The remainder of this paper is organized as follows. Section II describes the ANN modeling, Section III introduces the adder, subtractor and current mirror circuits. Section IV presents modeling and circuit simulation results. Finally, conclusions are drawn in Section V.

II. ANN MODELING

ANNs are an interconnection of a set of artificial neurons, with data processing ability. Each neuron in the network has a set of inputs, synaptic weights and bias. By proper training, an ANN can perform any kind of nonlinear modeling, provided that enough training data is available. Weights and bias are determined during the training phase, according to a specified performance goal. Fig. 1 shows the MLP network, which consists of one input layer, hidden layer(s), and one output layer. The input layer consists of sensory units connected to the outside environment. The hidden layer performs a projection of the input space into a hidden space through a nonlinear mapping. The output neurons then combines a weighted representation of the outputs from the previous layer, either in a linear or nonlinear fashion. Each neuron output y_i of the hidden layer in the MLP network is represented as

$$y_i = \text{sig} \left[\sum_{j=1}^n \sum_{k=1}^m x_j \cdot w_{kj} + b_i \right] \quad (1)$$

where $\text{sig}(\cdot)$ represents the sigmoid function, x_j denotes the input, w_{ij} is the synaptic weight connecting the i -th neuron in the hidden layer and the j -th input, and b_i is the neuron bias. A similar notation is applied to the output neuron

$$I_D = \sum_{k=1}^n y_k \cdot w_k + b \quad (2)$$

For transistor modeling purposes, the inputs ($m = 3$) of the ANN are defined as: the drain to source voltage (V_{DS}), gate to source voltage (V_{GS}), and transistor width (W). The output is the drain current (I_D). The ANN contains a single hidden layer. By means of training samples, the ANN can learn the physical process, subject to minimization of a cost function (mean square error - MSE). To attain best performance, a trail-and-error approach is used with different number of neurons in the hidden layer. The ANN model has been subsequently implemented in Verilog-A to create a generic cell, for circuit simulations at transistor level. Fig. 2 shows the TFT equivalent MLP network.

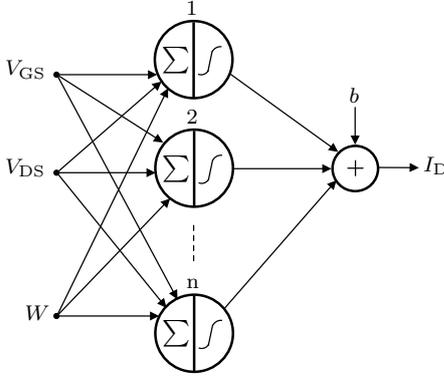


Fig. 1. Multi-layer perceptron.

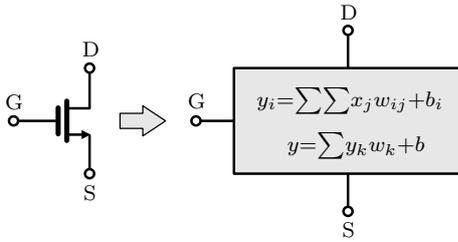


Fig. 2. TFT with ANN equivalent.

III. CIRCUITS

A. Subtractor/adder circuit

Analog subtractor and adder circuits are important functional blocks in computational systems. In Fig. 3, M_1 and M_2 TFTs form the subtractor, whereas M_1 – M_4 together form the adder. According to [5], in the saturation region, the drain current below and above threshold voltage is proportional to a power law of the gate voltage, respectively,

$$I_{Dsat,b} \propto V_{GF}^{\beta+2} \quad (3)$$

and

$$I_{Dsat,a} \propto V_{GT}^{\alpha+2} \quad (4)$$

where V_{GF} is the difference of the gate to the flat-band voltage while V_{GT} represents the difference between the gate voltage and the threshold voltage. The parameters α , β are constants related to the characteristic temperature of the tail and deep states, respectively.

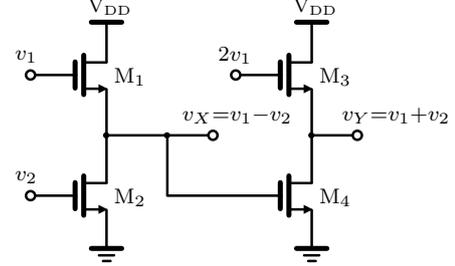


Fig. 3. Subtractor/adder circuit.

In order to attain the adding and subtraction operation, all the transistors are operated in saturation. The drain currents from M_1 and M_2 are then expressed as

$$i_{D1} = K [v_1 - v_X - V_T]^{\alpha+2} \quad (5)$$

$$i_{D2} = K [v_2 - V_T]^{\alpha+2} \quad (6)$$

Equating i_{D1} and i_{D2} due to series connection of M_1 and M_2

$$[v_1 - v_X - V_T]^{\alpha+2} = [v_2 - V_T]^{\alpha+2} \quad (7)$$

results

$$v_X = v_1 - v_2 \quad (8)$$

Applying the same analysis to M_3 and M_4 , one gets

$$[2v_1 - v_Y - V_T]^{\alpha+2} = [v_1 - v_2 - V_T]^{\alpha+2} \quad (9)$$

which simplifies to

$$v_Y = v_1 + v_2 \quad (10)$$

B. Current Mirror

Current mirrors are frequently used as active loads in integrated circuits. A simple current mirror is shown in the Fig. 4. From small-signal analysis, it is known that the output impedance R_{out} of the current mirror is equal to the output impedance of transistor M_1 . Since the transistors in this work have a of length $20\mu\text{m}$, impact of channel length modulation is not significant. So, the drain current of the transistor in the saturation region, is highly dependent on the gate to source voltage V_{GS} . For the transistors with the same length, the relation between input and mirrored current is given by

$$\frac{I_{out}}{I_{in}} = \frac{W_1}{W_2} \quad (11)$$

where W_1 , W_2 are the widths of the transistors M_1 and M_2 , respectively.

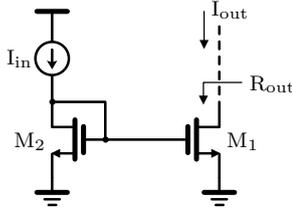


Fig. 4. Basic current mirror.

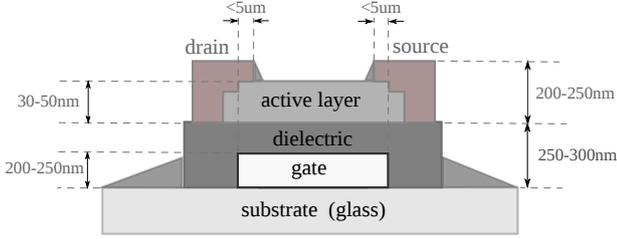


Fig. 5. TFT structure.

IV. RESULTS

A. Measurement Setup for Modeling

The a-GIZO devices used in this work are fabricated at FCT-UNL [2], [14]. RF magnetron sputtering, without intentional substrate heating, is used to fabricate all the layers of the oxide TFTs on glass substrates. The devices have a staggered bottom-gate structure, as shown in Fig. 5, with IZO gate, source and drain electrodes, a-GIZO with 2:4:2 Ga:In:Zn atomic ratio active layer and $\text{SiO}_2/\text{Ta}_2\text{O}_5\text{-SiO}_2/\text{SiO}_2$ multi-component/multilayer dielectric. The usage of this dielectric structure allows the transistors to exhibit a gate leakage current in the pA range, even if a low annealing temperature of 150°C is used here for the final devices [2]. The TFTs have a field-effect mobility of $\sim 20\text{cm}^2/\text{Vs}$, close to 0V turn-on voltage, on/off ratio exceeding 10^8 and a sub-threshold slope of $0.20\text{V}/\text{dec}$. Different width-to-length ratios were tested, with L being fixed at $20\mu\text{m}$ and W changing between $40\mu\text{m}$ and $320\mu\text{m}$. Measurements have been performed using a semiconductor parameter analyzer Keithley 4200-SCS, and probe station Cascade Microtech M150 under darkroom conditions.

B. Modeling

Matlab is used to train the MLP network with the measured data. The training samples are the drain current of the TFT as a function of V_{DS} , V_{GS} and W . The training data is formulated as follows: TFT widths of 40, 80, 160 and $320\mu\text{m}$; V_{DS} and V_{GS} in the range of 0 to 20V, in steps of 0.25V for the former and 2V for the latter. For all transistors, the lengths are kept equal to $20\mu\text{m}$. The resulting MLP-ANN has 50 neurons. Following the training and model implementation in Verilog-A, Cadence Spectre is used to obtain the I-V characteristics of the TFTs, as shown in Fig. 6. The blue circles represent training data for V_{GS} with a step size of 2V, whereas the red dots represent the testing data with 0.5V steps. The threshold voltage (V_{TH}) of

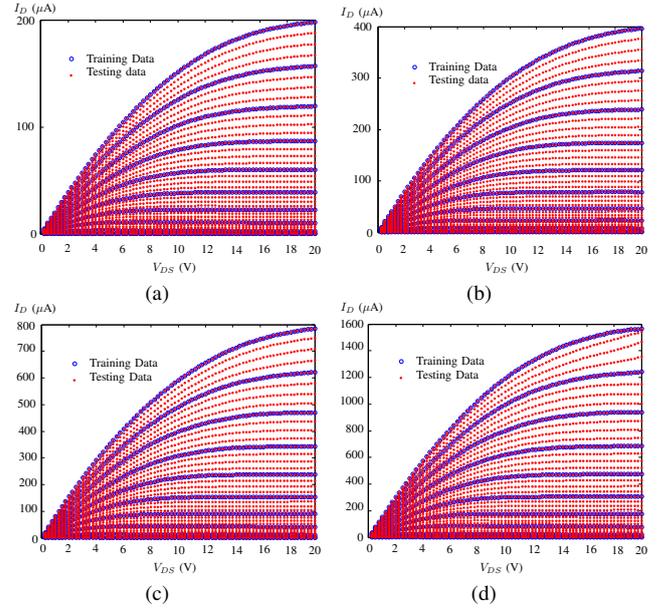


Fig. 6. ANN modeling results for device width of (a) $40\mu\text{m}$, (b) $80\mu\text{m}$, (c) $160\mu\text{m}$, and (d) $320\mu\text{m}$.

the TFTs are found to be $\approx 1.6\text{V}$. The widths are limited in the range of 40 to $320\mu\text{m}$, which correspond to the learning boundaries. Outside this region, extrapolation problems are expected. However, beyond the upper bound, this issue can be overcome by the simple method shown in Fig. 7, i.e. a parallel connection of transistors with sizes within the boundary.

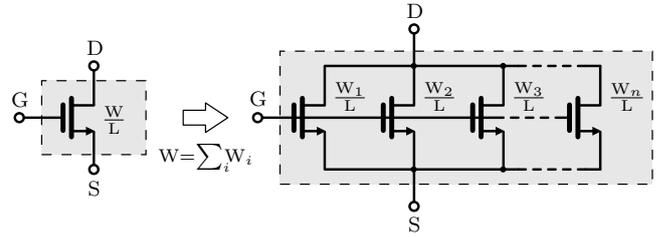


Fig. 7. Extrapolation for the TFT channel width.

C. Simulation of the analog building blocks

For the subtractor/adder circuit, the input stimuli are defined as

$$v_1(t) = 8 + \sin(\omega_1 t) \quad (12)$$

$$v_2(t) = 4.5 + 0.5 \sin(\omega_2 t) \quad (13)$$

whereas the power-supply in the circuit is 16V. The inputs were set to values that ensure saturation of all the transistors. The sizes of the TFTs were set with the same aspect ratios, i.e. widths of $40\mu\text{m}$ and lengths of $20\mu\text{m}$. The adder and subtractor outputs are compared against the functional results obtained from Matlab, for two different cases regarding the input frequencies: *i)* $\omega_1 = \omega_2$, and *ii)* $\omega_1 \neq \omega_2$. The results are shown in Fig. 8.

For the current mirror circuit, the value of the input I_{in} is swept from 100 to $200\mu\text{A}$. The two transistors have the same

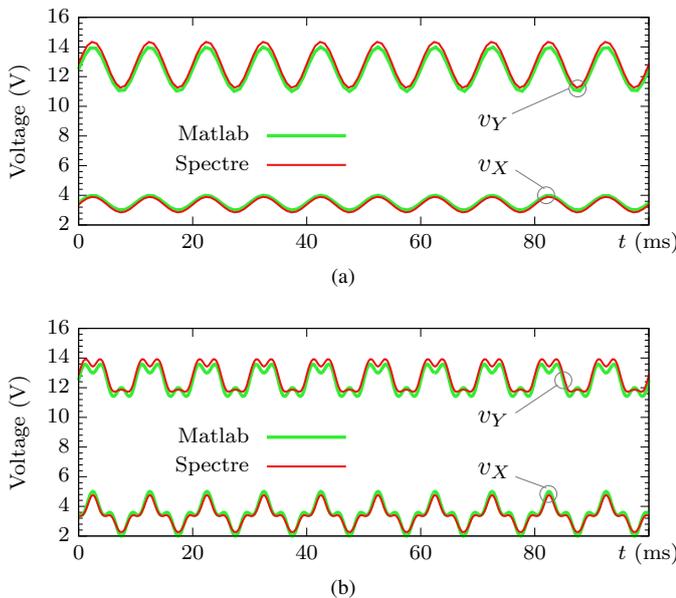


Fig. 8. Subtractor/adder outputs for (a) $\omega_1 = \omega_2 = 200\pi$ rad/s, and (b) $\omega_1 = 200\pi$ rad/s, $\omega_2 = 600\pi$ rad/s.

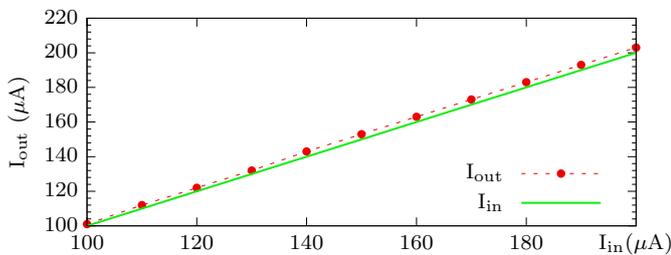


Fig. 9. Current mirror results.

width and length, respectively, 160 and $20\mu\text{m}$. The input and mirrored currents are plotted in Fig. 9. The slight difference between both is due to the drain current dependence on V_{DS} . The output resistance of the current mirror has been estimated in order of a few hundreds of $k\Omega$.

V. CONCLUSION

This paper discussed an MLP-ANN modeling approach for a-GIZO TFT devices, implemented in Verilog-A to enable the integrated circuits design in CAD environments. Transient and dc simulation results have demonstrated that the ANN model accurately predicts the device performance for static conditions and low-frequency operation. A subtractor/adder and current mirror have been successfully tested with the modeled devices, further demonstrating the capability of a-GIZO TFTs to operate with analog signals.

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