Multipliers with Transparent a-GIZO TFTs using a Neural Model

Ganga Bahubalindruni, Cândido Duarte, Vítor Grade Tavares,
Pedro Barquinha, Rodrigo Martins, Elvira Fortunato, and Pedro Guedes de Oliveira

***Abstract*—This paper presents the results of a preliminary study to examine the ability of post-silicon devices for analog processing. It is focused on the latest thin-film transistors (TFTs) with amorphous gallium-indium-zinc oxide (a-GIZO) as active layer. Three circuit configurations are presented: a differential pair and two multiplier topologies. Both triode and saturation regions of operation are included in the analysis, with the devices set to remain in strong accumulation. A neural model, which is developed based on the measured data of the TFTs, is used for the circuit simulations in the Cadence Virtuoso environment. The analog multipliers simulation results are compared against the expected functional results.**

***Index Terms*—a-GIZO TFTs, neural models, multipliers.**

I. Introduction

The amorphous gallium-indium-zinc-oxide (a-GIZO) thin-film transistor (TFT) technology is relatively new and it is mainly contemplated for large-area, low-cost transparent electronics, as the case of flat panel displays. Nonetheless, applications of this technology are not only confined to AMOLED [1] and AMLCD [2], but also extended to RFID tags [3] and sensors [4]. Two attractive features of this technology are low temperature fabrication and improved electrical characteristics, when compared to other TFT technologies. The a-GIZO TFTs can be fabricated at room temperature [5], with annealing temperatures not exceeding 150° C, which allows the use of a wide range of substrates like paper, glass and plastic. Regarding the electrical properties, a-GIZO TFTs are inferior when compared to standard CMOS transistors, since the semiconductor has an amorphous nature and because of this, the electron flow is limited by the trap states. However, it does exceed other existing TFT technologies. The mobility of a-GIZO TFT is $20\,\mathrm{cm^2/V{\cdot}s}$ [5], whereas the organic TFT mobility is $0.1\text{–}1\,\mathrm{cm^2/V{\cdot}s}$ [6] and a-Si:H TFT mobility is $1\,\mathrm{cm^2/V{\cdot}s}$ [7], which shows that a-GIZO TFT predominates over the organic and a-Si:H TFTs. Passive resistors can be realized and fabricated in a-GIZO TFT technology unlike organic semiconductor technology. There is a strong need of analog circuits for interfaces like sensors, filters, amplifiers, A/D and D/A converters, and power management circuits to realize a complete system. Given the advantages associated with the a-GIZO TFT technology, it is interesting to test the suitability of these TFTs for analog circuit design.

The lack of stable P-type TFTs and built-in libraries, for the active and passive elements with this a-GIZO technology, can be the limiting factors for analog circuit design. There is no extensive work reported towards analog circuit design with this technology, however driving circuits [8], ring oscillators [9], memories [10] and a 6-bit D/A converter were recently published [11].

In analog design, the differential pair represents a fundamental block in operational amplifiers. It is responsible for amplifying the difference of signals and acts as a suppressor of common-mode noise. Analog multipliers are also very important functional blocks and have diverse applications in communication systems, instrumentation functions, signal generators and filters. They are mostly confined to BJT, CMOS and BICMOS technologies. To the authors' knowledge, no analog multiplier was reported with any type of thin-film transistors so far. Various applications associated with differential amplifier and analog multipliers are motivating factors to characterize them with the TFT technology under discussion.

In order to design circuits, accurate device models are required, which can predict the device behavior in circuit simulations. As this a-GIZO TFT technology is an evolving one, there are no commercial models available, nevertheless few articles reported physical models [12]. In the present work, in order to simulate the circuits, we have developed a neural model from the measured data of the transistors [13] and implemented in Verilog-A. With this Verilog-A neural model, a differential amplifier and two different four-quadrant multipliers with a-GIZO TFTs are characterized by means of simulation. One multiplier is based on a four-transistor topology [14], operating in the triode region, and the other consists of a Gilbert-type cell working in saturation [15]. In all the circuits, the devices operate in the strong accumulation regime. The multipliers were not subjected to any particular optimization criteria, they just serve as purpose to analyze the ability of a-GIZO TFTs to perform analog signal processing.

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G. Bahubalindruni, C. Duarte, V. G. Tavares and P. G. de Oliveira are with INESC TEC (formerly INESC Porto) and Faculty of Engineering, University of Porto, Campus FEUP, Rua Dr. Roberto Frias, 378, 4200-465 Porto, Portugal. (email: vgt@fe.up.pt)

P. Barquinha, R. Martins and E. Fortunato are with the Materials Science Department, CENIMAT/I3N, Faculty of Sciences and Technology of New University of Lisbon and CEMOP/UNINOVA, Campus de Caparica, 2829-516 Caparica, Portugal. (email: pmcb@fct.unl.pt)

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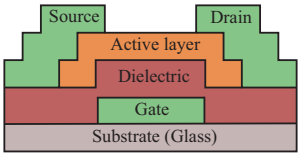

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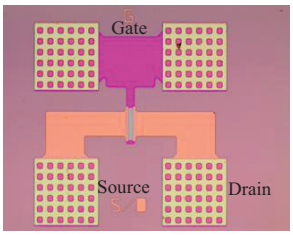


(b)

Fig. 1. (a) a-GIZO TFT structure, and (b) fabricated device.

Device structure

The TFTs used in this work are fabricated at FCT-UNL [16] with the structure shown in Fig. 1. They have an on/off ratio exceeding 10^8 and a sub-threshold slope of $0.20\,\mathrm{V/dec}$. They are fabricated on a 5 layer process (gate electrode, dielectric, oxide semiconductor, source/drain electrodes, passivation). Data measurements are obtained under darkroom conditions for TFT modeling with ANNs.

The rest of the paper is organized as follows. Section II presents the analysis of the analog circuits, and section III demonstrates the ANN modeling details and simulation results. Finally, section IV shows the conclusions.

II. Circuits for Analysis

Three circuit configurations are considered: a differential pair and two differential four-quadrant multipliers. In functional terms, the nonlinear behavior is fundamental to attest the viability of the technology for a broader-sense application in analog signal processing systems. Two differential multiplier configurations are considered in this study. One is attained from transistors working in the linear region, whereas in the other, the devices operate in saturation (Gilbert cell). This way the study is spanned through the different regions of transistor operation. For the analysis, the I-V relation for TFTs is roughly approximated to a FET, i.e. the drain current in linear and saturation regimes are expressed respectively as

$$i_{\mathrm{DS}} \approx K\big(v_{\mathrm{GS}} - V_{\mathrm{T}} - \tfrac{1}{2}v_{\mathrm{DS}}\big)v_{\mathrm{DS}} \tag{1}$$

and

$$i_{\mathrm{DS}} \approx \tfrac{1}{2}K(v_{\mathrm{GS}} - V_{\mathrm{T}})^2 \tag{2}$$

A. Differential pair

A single stage differential amplifier is shown in Fig. 2. From the large-signal analysis, it is known that the differential output current i_{OUT} is almost linear when the input voltages $v_{\mathrm{IN}} = V_{\mathrm{IN}} \pm v_{in}$ are within the range $\pm\sqrt{I_{\mathrm{SS}}/K}$, where K is the intrinsic transconductance of the TFT (including the aspect ratio W/L).

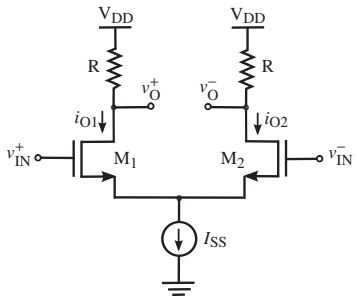


Fig. 2. Differential amplifier.

B. Multiplier I

The schematic of the first multiplier (hereon termed $\mathrm{MUL_I}$) is shown in Fig. 3a. In this circuit, $\mathrm{M_1}$ to $\mathrm{M_4}$ operate in the linear region, while $\mathrm{M_5}$ and $\mathrm{M_6}$ operate in saturation. They act as source followers that keep the voltage constant at their sources such that it can be treated as a virtual ground for signal. Denoting this voltage as V, the output current can then be defined as

$$i_{\mathrm{OUT}} = i_{\mathrm{O1}} - i_{\mathrm{O2}} \tag{3a}$$
$$= (i_1 + i_3) - (i_2 + i_4) \tag{3b}$$

where

$$i_1 \approx K([x^+ - y^+] - V_{\mathrm{T}} - \tfrac{1}{2}[V - y^+])\,(V - y^+) \tag{4a}$$
$$i_2 \approx K([x^- - y^+] - V_{\mathrm{T}} - \tfrac{1}{2}[V - y^+])\,(V - y^+) \tag{4b}$$
$$i_3 \approx K([x^- - y^-] - V_{\mathrm{T}} - \tfrac{1}{2}[V - y^-])\,(V - y^-) \tag{4c}$$
$$i_4 \approx K([x^+ - y^-] - V_{\mathrm{T}} - \tfrac{1}{2}[V - y^-])\,(V - y^-) \tag{4d}$$

from which results

$$i_{\mathrm{OUT}} \approx 2K\big([x^+ - x^-]\,[y^+ - y^-]\big) \tag{5}$$

C. Multiplier II

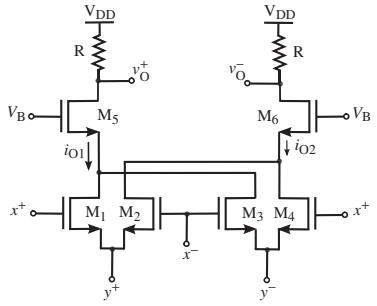
The Gilbert cell, which will be referred to as $\mathrm{MUL_{II}}$, takes advantage of the approximate linearity between the differential input voltage and the resulting differential output current to realize a multiplier. Fig. 3b shows an example built from three differential pairs.

The differential output current of the multiplier is given by

$$i_{\mathrm{OUT}} \approx Kx\left(\sqrt{\left[\sqrt{\frac{I_{\mathrm{SS}}}{K} - \frac{y^2}{2}} + \frac{y}{\sqrt{2}}\right]^2 - x^2}\right.$$
$$\left. - \sqrt{\left[\sqrt{\frac{I_{\mathrm{SS}}}{K} - \frac{y^2}{2}} - \frac{y}{\sqrt{2}}\right]^2 - x^2}\right) \tag{6}$$

where x and y are the differential input voltages. Assuming small x and y,

$$i_{\mathrm{OUT}} \approx 2Kxy \tag{7}$$



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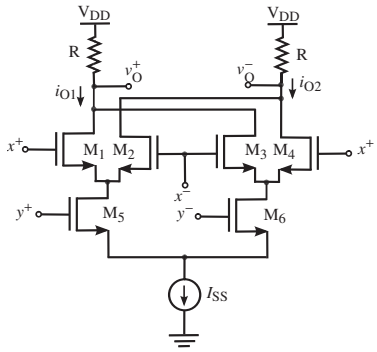

(b)

Fig. 3. Multiplier topologies: (a) MUL_I, and (b) MUL_II.

III. Results

A. ANN model and results

As a first step, a neural model is developed for the a-GIZO-TFT based on the measured data. Then this model is implemented in Verilog-A to create a generic cell so that it can be used in circuit simulations.

B. ANN modeling

A multilayer perceptron (MLP) network, trained with back-propagation (BP) algorithm, is used to model the measured drain current as a function of bias voltages V_{GS}, V_{DS} and aspect ratio W [13]. The input data to the ANN is as follows: V_{GS} and V_{DS} are in range of 0 to 20 V in steps of 2 V and 0.5 V, respectively. The W values are 40 μm, 80 μm, 160 μm, and 320 μm. All the data used is taken from measurements on a real transistor (Fig. 1). During training, the input data is divided into three parts in a random fashion, namely training data (60 %, this data is used to train the network), validation data (20 %, this data is used to check the ANN modeling performance for the unseen data during training; validation checks are used for stopping criteria during training) and testing data (20 %, this data is used to check the ANN generalization capability after training). Matlab 2011b is used to train the network. The network performance in terms of mean square error (MSE) is shown in Fig. 4. Post training regression plots are shown in Fig. 5, which shows that the model does predict well the device behavior, as the correlation factor is 1 and the error is very small.

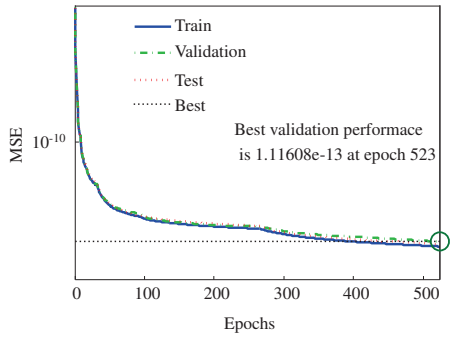

Fig. 4. ANN performance.

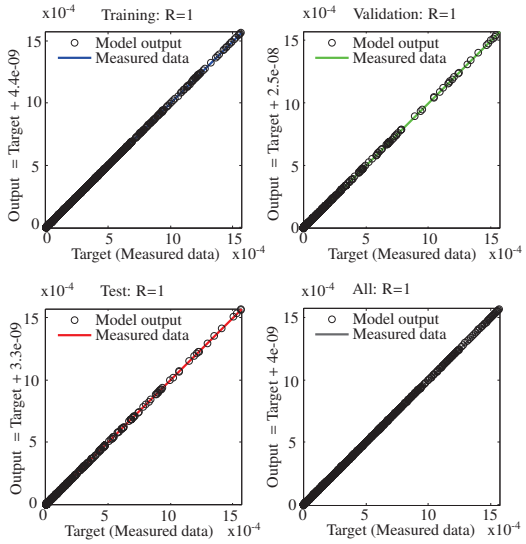

Fig. 5. ANN post-training performance.

Once the network met the required performance goal, from the measured data, the resulting ANN model (with 50 neurons) is implemented in Verilog-A to create a generic cell and this model is used in the following circuit simulations.

C. Circuit simulation results

For all experiments, the size of the a-GIZO TFTs are $80\,\mu\text{m}/20\,\mu\text{m}$, and the power supply is 16 V. The Cadence Virtuoso with the Spectre simulator is used to simulate the circuits. All tests are performed with the transistors in strong accumulation, and the analysis is confined to static behavior. The dc transfer characteristic of the differential amplifier is shown in Fig. 6 and the amplifier is almost linear in the range of ± 5.6 V as predicted by $\pm\sqrt{I_{SS}/K}$.

The following stimulus is applied to both multipliers for checking functional response

$$x = 10 \pm \sin(\omega_1 t), \quad y = 4 \pm \sin(\omega_2 t) \tag{8}$$

where ω_1 is 200π and ω_2 is 2000π. Both multipliers response are compared against the expected functional results from Matlab in normalized form as shown in Fig. 7. To check the TFT performance as a multiplier, its linearity response

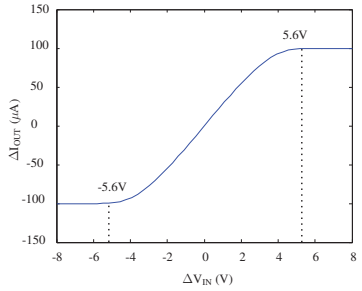

Fig. 6. Transfer characteristics of the TFT differential pair.

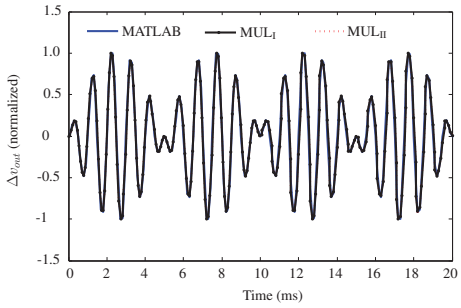

Fig. 7. Multiplier normalized functional response.

is confronted with the corresponding MOSFET version (in a 0.35 μm processes under identical conditions) and also with the expected ideal results, as shown in Fig. 8. The resulting linearity errors can be found in Table I at identical input conditions. The functional and linearity analysis results of the TFT multipliers show that they present a similar behavior to MOS conterpart, at least in functional terms.

IV. Conclusion

Post training regression plots show that the developed neural model, which is based on measured data of the TFTs, has good accuracy. This model is used to simulate a differential amplifier and two different multiplier topologies in Cadence Virtuoso environment. The multipliers simulation response is in good agreement with the expected functional behavior. The linearity response of the multipliers with TFT were compared with the corresponding MOSFET version, under identical conditions, just for control purposes. It shows that the linearity of the TFT multipliers is in the same order of magnitude as the MOSFET and follow the same trend, demonstrating that TFTs can be used to perform higher level functions.

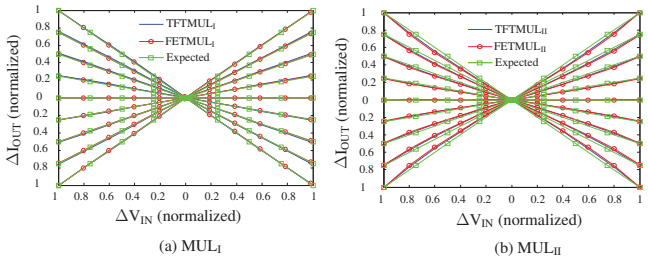

Fig. 8. Multiplier normalized linearity response.

TABLE I
Linearity Error.

Circuit	TFT	MOS
MIL_I	2.84%	0.44%
MIL_{II}	8.08%	10%

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