Design of a Current-Mode Class-D Power Amplifier in RF-CMOS

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***Abstract*—The present paper addresses the implementation of a radio-frequency power amplifier operating in current-mode class-D. In particular, this paper focuses the technical issues concerning the design of a fully-integrated version of the amplifier in a RF-CMOS technology. It is demonstrated that the parasitic series resistance of an integrated load inductor has great impact in the drain efficiency value. In order to compensate for this effect, the reduction of the load network Q_L has been adopted. A RF-CMCD power amplifier has been designed in 90-nm CMOS including all the inductors on-chip. Simulation results demonstrate 76% drain efficiency, for up to 16-dBm output power at 2.45-GHz operation frequency.**

***Index Terms*—CMCD, power amplifiers, CMOS, RF, wireless communications, ISM band.**

I. Introduction

The power amplifier is the most critical circuit in any wireless transmitter. The major bottleneck is found in achieving high power-efficiency, which has a large impact in communication time and also in battery lifetime for portable wireless devices. Besides the high-efficiency concern, modern mobile communication systems also demand cheap and reliable technologies. Submicron CMOS has already proven its feasibility for implementation of RF circuits beyond the GHz range [1], [2]. Moreover, due to the typical large-scale density of CMOS circuits, the digital baseband and RF circuits can be both integrated on the same die, thus providing a low-cost and fully-integrated solution.

A. Switching-mode power amplifiers

Typically, conventional linear power amplifier classes such as AB and B exhibit poor efficiency values. Switching-mode amplifiers overcome this issue, because theoretically can provide 100% drain efficiency. There are two main types of power losses that can be commonly identified in these classes: conduction and switching losses [3]. The conduction losses are due to the finite ON resistance of the non-ideal switch and is generally minimized by using very wide transistors. On the other hand, large transistors imply large shunt capacitances, which are responsible for the switching losses. At the OFF-ON transition, the energy stored in the parasitic capacitance is discharged through the transistor. Therefore, the amount of energy given by $\frac{1}{2}CV^2$ is lost every switching cycle. As a result, switching losses can be the dominant factor in the efficiency of high-frequency switching amplifiers. Among the most power-efficient architectures, class-E and current-mode class-F are widely popular. In these classes, the turn-on instant occurs at the time when the switch parasitic capacitance is completely discharged. This condition is commonly known as zero-voltage switching (ZVS) and can effectively minimize the switching losses. In other classes, such as the conventional voltage-mode class D (VMCD), the ZVS condition cannot be met. In fact, VMCD only has 100% theoretical efficiency if the switches shunt capacitances are neglected. As in the class-F, the class-D can minimize the effect of the parasitic inductance of the transistor drain terminal. This is due to the zero-current switching condition (ZCS) present in voltage-mode classes [4]. However, ZCS condition is less significant in fully-integrated amplifiers since the series parasitic inductances of the transistors are generally reduced.

Figure 1 depicts the basic circuit of the current-mode class-D (CMCD) [4]–[9]. It is the dual version of the VMCD. Operating in the current domain, the CMCD architecture alleviates the problem of parasitic discharge by imposing the ZVS condition. Power amplifiers designed for this class are suitable for high output-power applications with good drain efficiency. Table I summarizes some existent implementations of CMCD power amplifiers. As can be seen, drain efficiency results are in the range of 60% up to values similar to the theoretical maximum drain-efficiency in class B, *i.e.* approximately 79%. Different technologies have been used in CMCD implementations, most of them based in III-V semiconductors. These works refer relatively

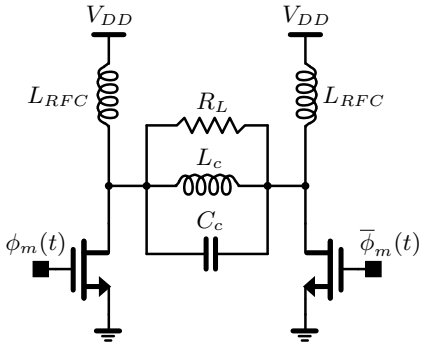


Figure 1. Circuit of the CMCD power amplifier.

Table I
CMCD EXISTENT RF IMPLEMENTATIONS.

Ref.	f (GHz)	η_D (%)	P_{out} (dBm)	Technology
[4]	0.9	76.3	24.6	GaAs FET
[6]	0.7	78.5	29.5	GaAs HBT
[7]	1.0	65.4	36	GaN HEMT
[8]	0.9	75/78	43.2/47.1	GaN MESFET
[5]	1.0	60	41.1	LDMOS
[9]	1.0	71	43.1	LDMOS

different levels of output power but in the same frequency range, around 1-GHz. However, at the present time, implementations of the CMCD power amplifier in Si-CMOS are yet unknown.

This work reports the CMOS implementation of the CMCD amplifier for RF applications, in the 2.4-GHz ISM band. Although the switching losses are avoided by the CMCD configuration, the on-chip implementation of all components introduces more loss sources, particularly due to the integrated inductors that have typically low quality factors in RF-CMOS technologies. This paper is organized as follows. First, the basic concept of the CMCD is briefly described, following an analysis of non-ideal characteristics of the load network and its influence in the CMCD operation. Simulation results of a CMCD power amplifier designed in a 90-nm CMOS technology is then presented.

II. BASIC CONCEPT OF THE CMCD ARCHITECTURE

The basic architecture for a CMCD power amplifier, represented in Figure 1, is comprised of two RF chokes (L_{RFC}) that act as current sources. The load network is tuned at a central frequency:

$$\omega_c^2 = \frac{1}{L_c C_c} \tag{1}$$

with the quality factor Q_L of the load network given by:

$$Q_L = \frac{R_L}{\omega_c L_c} \tag{2}$$

where R_L is the resistive load representing the antenna, typically 50Ω. Both transistors operate as switches driven by a square wave 180 degrees out-of-phase. The current flowing in the load network is a square waveform with null DC value. Ideally, there are no voltage harmonics

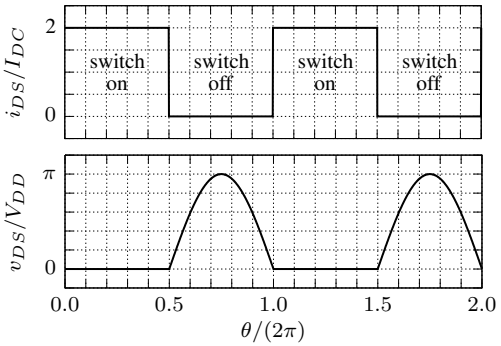


Figure 2. CMCD ideal voltage and current waveforms in a switch.

besides the fundamental tone, because the LC filter short-circuits the resistive load R_L for any frequency other than the fundamental one. Consequently, the differential voltage taken at the drains of the transistors is a sinusoidal waveform.

Since the RF chokes define the DC voltage V_{DD} at each drain, the peak voltage value is given by $\pi \cdot V_{DD}$. Figure 2 shows the ideal waveforms for one of the switches of the CMCD amplifier. The transistors turn-on when the corresponding drain voltage is null. Ideally, the switches only have voltage across them or current flowing through, never both. This non-overlapping feature of voltage and current leads to 100% of theoretical efficiency. The output power at the fundamental of the CMCD can be expressed as:

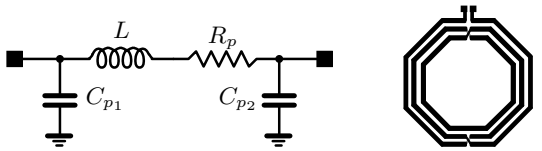
$$P_{out} = \frac{\pi^2}{2} \cdot \frac{V_{DD}^2}{2} \tag{3}$$

which is $\pi^4/4$ higher than its counterpart, the VMCD.

One key feature of the CMCD is that the parasitic shunt capacitance can be absorbed in the load capacitance C_c, thus providing a way to accurately ensure the ZVS condition. Another advantage of the CMCD power amplifier is its low peak voltage, *i.e.* $\pi \cdot V_{DD}$. Other ZVS architectures, like class E amplifiers, have relatively higher peak voltage values. This is a relevant factor in terms of reliability, since CMOS sub-micron devices have very reduced breakdown voltages.

III. ANALYSIS OF THE CMCD LOAD NETWORK

In this section, we present a mathematical analysis addressing the influence of the integrated load network on the CMCD operation. In RF-CMOS technologies the on-chip inductors have poor performance due to its low quality factors, typically less than 20. Figure 3(a) shows the electrical model of an integrated inductor. It is composed by the inductance L, its series parasitic resistance R_p, and the associated parasitic capacitances C_{p_1} and C_{p_2}. These two capacitances are approximately equal in the case of symmetrical inductors, such as the one represented in figure 3(b). Moreover, the inductance from each port is equal for differential inductors, due to symmetry. It should be noted that the parasitic capacitances of the inductor can also be absorbed by the load



(a) Electrical model. (b) Differential geometry.

Figure 3. On-chip inductor.

capacitance value. However, as described next, R_p can have significant effect in the load network impedance.

While for ideal inductors the resistance of the load network at the fundamental component is not influenced by the value of the load quality factor Q_L, *i.e.* it is always given by R_L, when considering the non-null value of R_p the real part of the impedance of the RLC tank is strongly affected by both parameters, Q_L and Q_u. In fact, the real part of the load impedance comprising of R_L, C_c and the non-ideal L_c with R_p can be expressed as R_{L_1} given as:

$$R_{L_1} = R_L \cdot \frac{Q_u\left(Q_L + Q_u\right) + 1}{\left(Q_L + Q_u\right)^2 + 1} \tag{4}$$

where the unloaded quality factor of the on-chip inductor is given by:

$$Q_u = \frac{\omega_c L}{R_p} \tag{5}$$

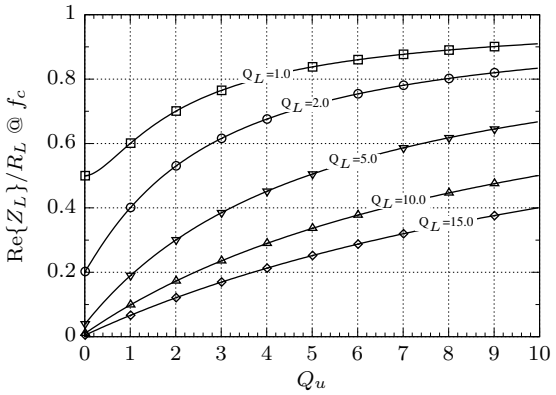
Equation (4) is plotted in figure 4(a) for different values of Q_L and Q_u. It is interesting to note that for a finite Q_u, increasing the value of Q_L effectively reduces R_{L_1}. However, due to the non-ideal quality factor values of Q_u and Q_L, the harmonic content increases. Based on (4), one can derive the ratio between the total power produced at the non-ideal RLC network (P_{DC}) and the power at the fundamental frequency also at the RLC network (P_1):

$$\frac{P_1}{P_{DC}} = \frac{|I_1|^2 R_{L_1}}{\sum_k^\infty R_{L_k}|I_k|^2} \tag{6}$$

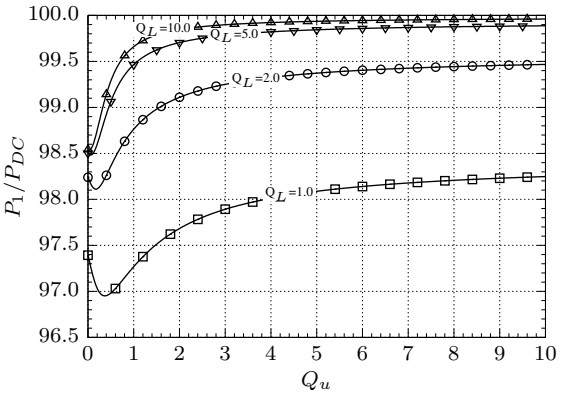
$$= \frac{R_{L_1}/R_L}{\sum_{k\ \text{odd}}^\infty \frac{Q_u(Q_L+k^2Q_u)+1}{k^4(Q_L+Q_u)^2+k^2[Q_LQ_u(k^2-1)-1]^2}} \tag{7}$$

where I_k in (6) is the *k*-th harmonic of the current in the RLC tank. From (7), which is plotted in figure 4(b), one can conclude that for non-ideal values of Q_u and Q_L commonly found in practice, the power is highly concentrated at the fundamental component, at least 97%, even with lower values of Q_L. The output power at the fundamental component in the load R_L can be expressed in a normalized form by the following function:

$$F(Q_L, Q_u) = \frac{1 + Q_u^2}{1 + \left(Q_L + Q_u\right)^2} \tag{8}$$



(a) Effect of Q_u and Q_L in the equivalent resistance at $f = f_c$.



(b) DC power and power at the fundamental frequency.

Figure 4. Effect of finite values for Q_u and Q_L in the CMCD.

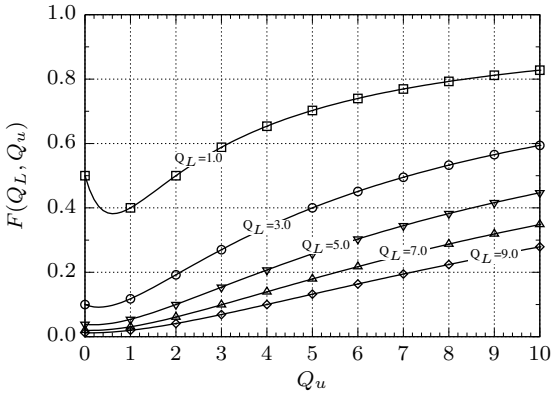
that is obtained from the fundamental component of the current flowing through R_L, as $\frac{1}{2}R_L|I_{1,R_L}|^2$. The value of the output power is given by:

$$P_{out} = \frac{8R_L I_p^2}{\pi^2} \cdot F(Q_L, Q_u) \tag{9}$$

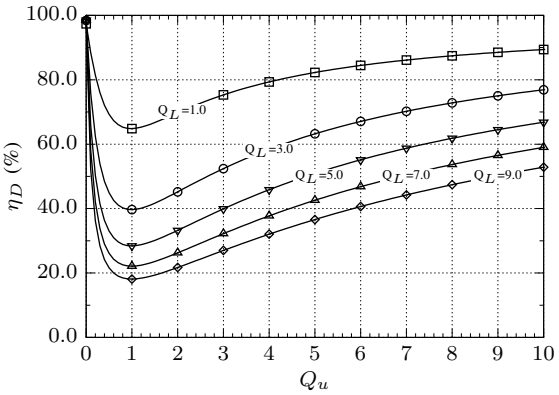
where I_p is the value of the DC current from each RF choke. The efficiency can also be written in terms of $F(Q_L, Q_u)$ as follows:

$$\eta_D = \frac{F(Q_L, Q_u)}{\sum_{k\ \text{odd}}^\infty \frac{1}{k^2} \cdot \frac{Q_u(Q_L+k^2Q_u)+1}{k^2(Q_L+Q_u)^2+[Q_LQ_u(k^2-1)-1]^2}} \tag{10}$$

Figure 5 shows the output power and drain efficiency in terms of Q_u and Q_L. It can be verified that low values of Q_L can be actually beneficial. Since in practice a non-finite Q_u exists, the use of low Q_L can be seen almost as mandatory in order to keep efficiency at reasonable values. As seen in figure 5(b), for low values of Q_u the power losses in the load network can effectively dominate the performance of the amplifier in terms of drain efficiency. In order to isolate the effect of the non-ideal load network in efficiency, the ON resistances of the switches have been neglected. The simulations presented in the following section will take into account also the switching losses and conduction losses due to finite ON

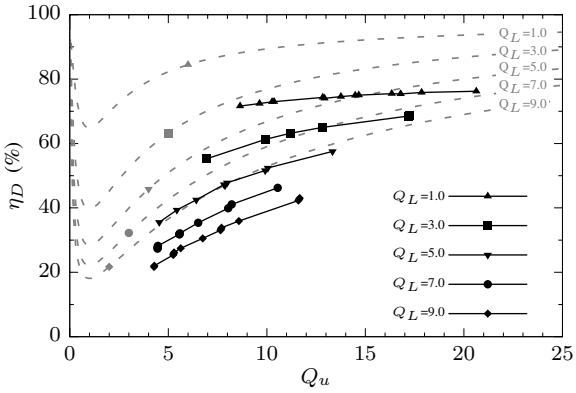


(a) Normalized fundamental power at the load R_L.

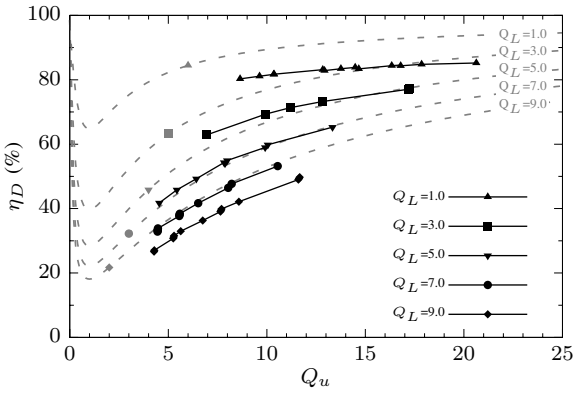


(b) Drain-efficiency.

Figure 5. Effect of finite values for Q_u and Q_L in the CMCD power and efficiency.



(a) Simulation with technology models of all on-chip inductors.



(b) Simulation with ideal chokes and load on-chip inductor.

Figure 6. Simulation waveforms for drain-efficiency with the technology models of on-chip inductors (solid lines) and the estimated efficiency from the theoretical analysis (dashed lines).

resistance, together with influence of the non-ideal load network.

IV. Results

To validate the low Q_L approach, a CMCD power amplifier (Figure 1) has been designed in a RF-CMOS process of 90-nm feature size. Simulations were performed with Cadence Virtuoso/MMSIM. A maximum efficiency of 76% with transmit power of 16-dBm was obtained at 2.45-GHz. The high performance of the PA was achieved increasing the inductor size and lowering C_c by the same factor, thus maintaining the RLC filter tuned at the central frequency. Therefore, it results a smaller quality factor Q_L and, in fact, the low quality factor of the load network increases the amplifier efficiency as seen previously. Improvements of more than 30% in efficiency can be readily observed by lowering Q_L. One can say that, since the load network loss mechanism has been minimized, the dominant power losses of the amplifier are now due to switching and conduction losses. This is a trade-off that must be accomplished to optimize efficiency of the amplifier.

Figure 6 shows the efficiency values obtained for several technology inductors (solid lines), each one with a different Q_u, and for various values of Q_L. In figure 6(a) it are shown the simulation results using on-chip inductor models for both the RLC filter and the RF chokes. In order to distinguish the impact of non-ideal chokes, figure 6(b) presents the efficiency results obtained replacing the on-chip chokes by ideal inductors. As can be seen, the non-ideal characteristics of the on-chip chokes can lower drain efficiency by 5–10%. The dashed lines in both pictures represent the theoretical efficiency, which is obtained from equation (10) of the previous analysis. Since the analysis does not take into account power losses other than in the non-ideal on-chip inductor, there is a noticeable offset in the value of the plotted efficiencies. Apart from this offset, which is due to non-ideal switches, one can observe similar curves behavior in both plots.

V. Conclusion

The design of CMOS CMCD power amplifier has been presented. The non-ideal characteristics of the load network have been identified as an important power loss contribution that leads to noticeable efficiency degradation. The use of a low quality factor network can effectively reduce these power losses. A CMCD power amplifier has been designed in 90-nm technology, achieving 76% maximum drain efficiency, with 16-dBm of output power at 2.45-GHz, using solely on-chip components.

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