Circuits for Analog Signal Conditioning with a-GIZO Transparent TFTs

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***Abstract*—This work aims to study the feasibility and limitations of amorphous Gallium-Indium-Zinc-Oxide (a-GIZO), thin-film transistor (TFT) technology for analog circuit design. In order to design and simulate circuits with these devices, a model has been developed using artificial neural networks and implemented in verilog-A for circuit simulation. The model validation and the a-GIZO TFT capability to perform signal processing operation are demonstrated with a multiplier circuit simulation, using the developed ANN model.**

I. Introduction

Among other non-silicon semiconductors, amorphous Gallium-Indium-Zinc-Oxide (a-GIZO) thin film transistors (TFTs) are gaining significant importance, mainly due to their improved electrical characteristics [1] and low temperature fabrication [2]. Consequently, a collection of different substrates can be used, such as paper, plastic or glass, allowing the construction of flexible and transparent electronic devices with exceedingly competitive prices. Applications with this technology have been confined to the active matrix displays [3] and driving circuits [4], whereas no extensive results have been reported on analog integrated circuit design. This work explores the ability of the a-GIZO TFTs for analog circuit design, specifically for signal conditioning and processing. This objective is achieved in three steps: (i) development of a device model, (ii) circuit design and simulation, and (iii) fabrication and test.

A. Device structure

The devices used in this work are fabricated at FCT-UNL and follow a structure shown in Fig. 1. The source, drain and gate electrodes are made up of IZO, a-GIZO is the active layer and SiO_2/Ta_2O_5-SiO_2/SiO_2 is the dielectric, an option taken to reduce the gate leakage current to the pA range [2], [5]. The TFTs have a field-effect mobility of $\sim$20cm^2/Vs.

The rest of the paper is organized as follows: section II describes the TFT modeling, section III shows a circuit design example, simulations and fabrication details and finally some conclusions are presented in section IV.

II. TFT modeling

Accurate device models are essential for an effective design flow of circuits. Generally, modeling methods can be categorized into physical, table based, semi-empirical and empirical. Physical models [6] are recognized as precise, but the development time is quite high. Alternatively, table-based models [7] demand huge data storage along with interpolation algorithms, and the accuracy of the semi-empirical and empirical models [8] can be limited. An evolving technology demands a simple, continuous and accurate device model that takes little time to develop, if circuit design is to be taken simultaneously. Artificial neural networks (ANNs) encompass many of these properties, representing a good modeling alternative under such constrains, and has already been applied successfully to MOSFET modeling, firstly by Litovski [9]. The development time, accuracy and capability to model the complete behavior of the device are the motivating factors that make ANNs as the primary choice of modeling in the present work, where circuit design is the ultimate goal.

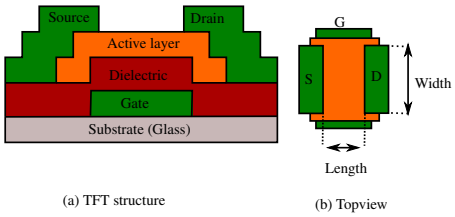
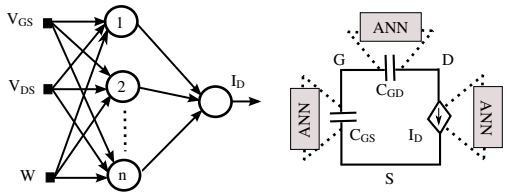


Fig. 1: a-GIZO thin film transistor

A multilayer perceptron (MLP) network, trained with back-propagation (BP) algorithm, is used to model the drain current as a function of bias voltages V_{GS}, V_{DS} and aspect ratio, as shown in Fig. 2a. Once the network meets the required performance goal, from the measured data, the resulted ANN model (with 50 neurons) is implemented in Verilog-A to create a generic cell for circuit simulations. In order to include the dynamic behavior of the device, bias dependent capacitances should be modeled similarly to the drain current. As the substrate is an insulator (glass), there is no bulk capacitance. So, the equivalent circuit employed for modeling is that shown in Fig. 2b.



(a) ANN topology (b) TFT equivalent

Fig. 2: ANN topology and device equivalent

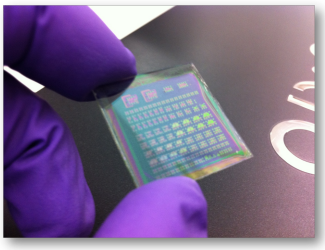


Fig. 5: The transparent chip

III. Circuit design

Various circuits have been designed and simulated with Cadence Spectre using the developed model, including different types of current mirrors, subtractor, adder, multiplier, single-ended common-source amplifier with diode connected load, differential amplifiers, and amplifiers with bootstrapping and cascoding techniques. One should be aware that no stable p-type devices are yet available for the current technology, which restricts all these circuits to n-type transistors. To show the feasibility of TFTs for analog circuits as well as the compatibility of the model for circuit simulation, a multiplier circuit [10], shown in Fig. 3, has been simulated in Cadence environment and confronted with the behavioral, expected result. Fig. 4 shows the result (normalized) for the following stimuli,

$$x = 9 \pm \sin(2100\pi t); y = 5 \pm \sin(400\pi t) \qquad (1)$$

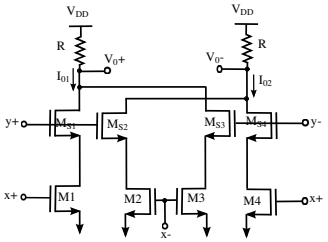


Fig. 3: TFT multiplier

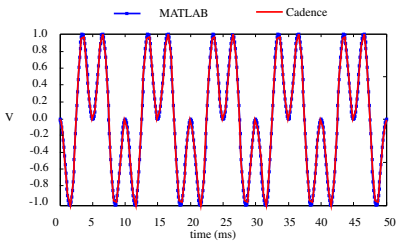


Fig. 4: Functional verification

The first transparent chip has been recently fabricated with all the aforementioned circuits (Fig. 5).

Conclusion

Simulation results are demonstrating that the ANN model is compatible with regular electric simulation and does not present severe convergence problems. The next step in this work is to characterize the dynamics of the a-GIZO transistor and test the real circuits to definitely validate the simulation results.

Acknowledgment

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