# High-Gain Topologies for Transparent Electronics

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***Abstract*—Transparent TFT technologies, with amorphous semiconductor oxides are lacking a complementary type transistor. This represents a real challenge, when the design of high-gain amplifiers are considered, without resorting to passive resistive elements. However, some solutions do exist to overcome the lack of a p-type transistor. This paper then presents a comparison analysis of two high-gain single-stage amplifier topologies using only n-type enhancement transistors. In these circuits, high gain is achieved using positive feedback for the load impedance. The comparison is carried out in terms of bandwidth, power consumption and complexity under identical bias conditions. Further, the same load impedance is used to develop a novel high-gain multiplier. All the circuits are simulated using a 0.35 $\mu$m CMOS technology, as it is easy to test the reliability of the methods, since CMOS transistors have trustworthy models.**

***Index Terms*—High gain amplifiers, Transparent electronics, Multipliers.**

## INTRODUCTION

Semiconductor oxide thin-film transistors (TFTs) technologies, such as a-GIZO and ZnO, are becoming attractive in various industrial applications. These technologies are mainly intended for the display [1] and backplane systems. However, they are gaining significant importance in other electronic applications such as RFIDs [2]. The most appealing factor that is bringing increasing attention to these emerging technologies is the ability to fabricate devices at room temperature. It extends the possible range of substrates such as paper or plastic, and facilitates the assembly of flexible electronics [3], [4], with foreseen impact in biomedical applications such as smart skin [5] as well as in signal processing and conditioning circuits. However, analog circuit design is still incipient and very limited, mainly because no stable p-type device is yet available. Hence, the circuit design must be confined to only n-type transistors. Nevertheless, few circuits have already been reported [6], [7], [8].

High gain stages are crucial blocks in operational amplifiers. When a simple common-source (CS) amplifier is considered in CMOS technology, high gain can be obtained by employing a p-type transistor as an active load with an n-type driver transistor. In case of depletion transistor technology, such as GaAs MESFET, the n-type transistor (gate connected to source) can be used as an active load to realize high gain [9]. However, depletion technology requires one additional mask, when compared to the enhancement counterparts [10]. Since a stable p-type transistor is not expect to emerge soon, overcoming the design challenges with the enhancement n-type transistor technology will certainly result in cost effective circuits.

When amplifiers need to be designed only with n-type enhancement transistors, the simplest load is a passive resistor. If the technology cannot realize passive resistors, a diode connected transistor is a viable option. For a simple CS amplifier with the diode connected load, gain depends on the aspect ratio of the driver and load transistors. In order to realize high gain with this topology, the driver transistor must have a high aspect ratio with respect to the load. Then, these stages can be cascaded to achieve high gain. However, this method penalizes the amplifiers bandwidth because of more delay stages. Alternatively, high gain can be designed by bootstrapping the small-signal level of the gate-source voltage of the load transistor, keeping the transistor in saturation [11].

In this paper, two different bootstrapping techniques [12], [13] are analyzed and their performance is compared in terms of bandwidth, power consumption and complexity. Apart from analyzing amplifiers, a basic Gilbert type cell [14] is also implemented using only n-type enhancement transistors in two ways. One method employs diode connected transistor as the load and the second method uses positive feedback to achieve a high load impedance. This is a novel high-gain multiplier with only n-type enhancement transistors.

The rest of the paper is organized as follows. Section I presents different amplifier topologies with n-type enhancement transistor. Section II shows the proposed high-gain multiplier. Section III demonstrate the simulation results and finally section IV gives the conclusions.

## I. AMPLIFIER TOPOLOGIES

When depletion or complementary type transistors are not available, the conventional loads to implement a simple CS amplifier could be a resistor ($R_L$) or a diode connected transistor as shown in Fig. 1(a) and 1(b) respectively. In order to realize high gain with the passive resistor as a load, a high value of resistance should be used, which consumes more chip area and requires high supply voltage. The other conventional

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alternative is the CS amplifier with a diode connected load. This circuit is referred as Amp1 from now on. The load resistance ($R_{oAmp1}$) of Amp1 is $\frac{1}{g_{m2}}$ and its small signal gain is given by,

$$\begin{aligned} A &= \frac{v_{out}}{v_{in}} \\ &\approx \frac{gm_1}{gm_2} \\ &\approx \sqrt{\frac{W_1/L_1}{W_2/L_2}}. \end{aligned} \quad (1)$$

When the driver and load transistors have the same length, the respective gain can be expressed as

$$A = \sqrt{\frac{W_1}{W_2}}. \quad (2)$$

In order to obtain a high gain, $W_1$ must be very large compared to $W_2$, which is not a practical solution. The bandwidth of the Amp1 is given by

$$BW_{Amp1} = \frac{1}{R_{oAmp1}(c_{gs2} + c_{gd1})}, \quad (3)$$

where $c_{gs2}$ is the gate to source capacitance of T2 and $c_{gd1}$ is gate to drain capacitance of the of T1 in Fig. 1b.

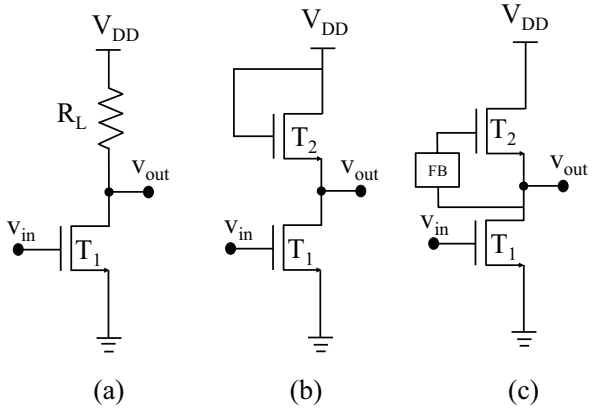


Fig. 1: Common source amplifier with : (a) Resistive load (b) Diode connected transistor load (c) High gain topology

Fig. 1(c) shows an alternative topology to achieve high gain with positive feedback. Its small signal equivalent circuit is shown in Fig. 2. By applying KCL at $v_{out}$ results in

$$\begin{aligned} v_{out}(g_{ds1} + g_{ds2}) + g_{m1}v_{in} + (1 - A_f)g_{m2}v_{out} = 0 \\ A = \frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{(1 - A_f)g_{m2} + g_{ds1} + g_{ds2}}. \end{aligned} \quad (4)$$

where, $A_f$ is the feedback circuit gain.

By making $A_f$ close to one, a high equivalent impedance results, greatly increasing the gain. To guarantee a stable behavior, $A_f$ must be less than unity. Circuits shown in Fig. 3 present two different forms of positive feedback that builds up the gain. The topologies shown in Fig. 3(a) and Fig. 3(b) are referred as Amp2 and Amp3 respectively. In Amp2, T1 and T2

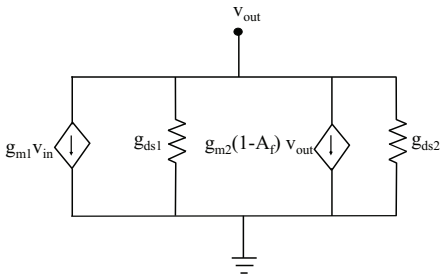


Fig. 2: High gain amplifier small signal equivalent

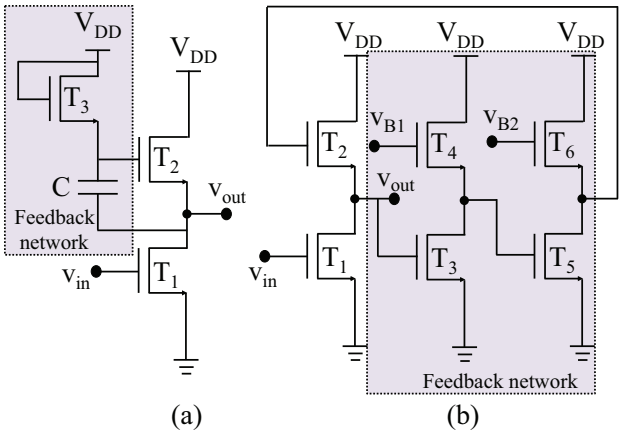


Fig. 3: Amplifier topologies for high gain: (a) Bootstrapping with capcitors and cutoff transistor (Amp2) [12] (b) Two stage inverting buffers (Amp3) [13]

operate in saturation, while T3 operates in cutoff. From small signal analysis, T2 gate is almost short-circuited to the source (when C is significantly higher than the parasitic capacitance of T3). For this topology, the gain and bandwidth depends on the value of C and the dimensions of the cutoff transistor (T3). Fig. 4(a) shows the same circuit taking in consideration the intrinsic capacitors. Note that neither $c_{db}$ nor $c_{sb}$ are considered because the bulk of TFTs is in fact an insulator. The equivalent capacitance ($c_{eq}$) at the output node of Amp2 is shown in Fig. 4(b). When C is very large compared to the transistors intrinsic capacitors, $c_{eq}$ is given by (5). Since T3 in Amp2 operates in cutoff, $c_{gs3}$ is nothing but the overlap capacitance between gate and source.

$$c_{eq} \approx c_{gd1} + c_{gd2} + c_{gs3} \quad (5)$$

A high-pass filter action is observed in Amp2 due to the feedback network (C and T3). Even though the lower cutoff frequency can be made very small, this circuit cannot amplify dc signals. The bandwidth of Amp2 is then given by

$$BW = \frac{1}{R_o c_{eq}}. \quad (6)$$

where $R_o$ is

$$R_o = \frac{1}{(1 - A_f)g_{m2} + g_{ds1} + g_{ds2}}, \quad (7)$$

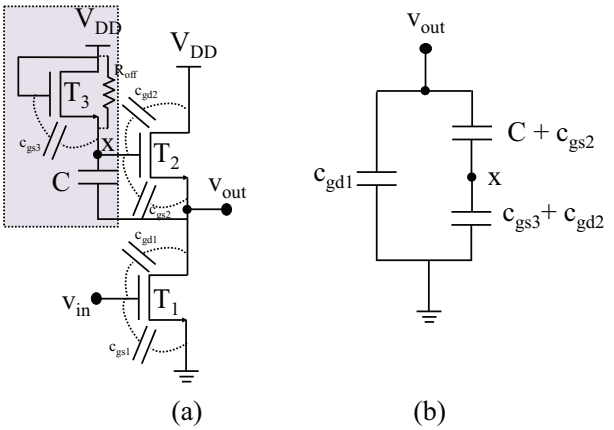


Fig. 4: Amp2: (a). Capacitors contributing for frequency response (b). Equivalent capacitance at the ouptut node

and $c_{eq}$ is given by (5). Amp2 is always stable as the feedback gain ($A_f$) is always less than one for this topology.

Amp3 employs two delay stages in the feedback network. This circuit can amplify dc signals, as there is no high-pass filter action in the feedback network. However, this feedback circuit causes lower bandwidth and higher power consumption. In this topology, transistors (T3 to T5) dimensions influence both the gain and bandwidth. All transistors in Amp3 operate in saturation and its bandwidth is given by,

$$\begin{aligned} \omega_f &= \omega_o(1 - A_f.A_2) \\ A_2 &= \frac{g_{m2}}{g_{m2} + g_{ds2}}. \end{aligned} \tag{8}$$

where $\omega_o$ is the open loop bandwidth. Its derivation using time constant method is shown in appendix. $A_2$ is the source follower (T2) gain in Fig. 3(b) and $A_f$ is the feedback gain. In order to ensure stable operation for Amp3, the feedback loop gain ($A_f.A_2$) must always be less than one.

## II. Multipliers

The traditional Gilbert cell with MOSFET version is shown in Fig. 5. Again the load ($R_L$) can be realized by a passive resistor or diode connected transistor, when complementary or depletion transistors are unavailable. In order to enhance the gain of the multiplier, the positive feedback concept can be adopted in a differential configuration as shown in Fig. 6. The multiplier in Fig. 5 with a diode connected transistor load is referred as Mul1 and Fig. 6 is referred as Mul2. During the small signal analysis of Mul2, the signal value at gate and source can be made equal for the transistors (T7 and T8), by employing proper bias and aspect ratio of the transistors in the feedback network formed by T9 to T13.

Again, Mul2 ensures higher gain at the cost of bandwidth and higher power consumption compared to the Mul1 because of the additional transistors in the positive feedback network.

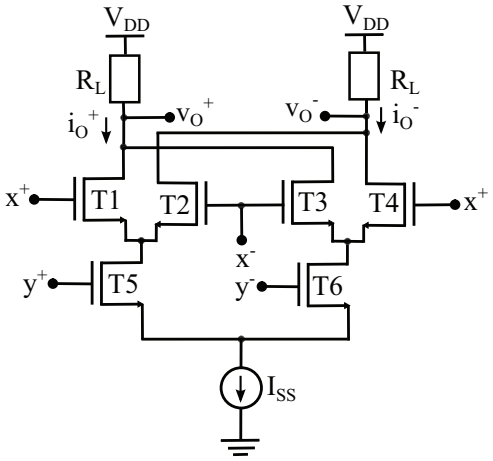


Fig. 5: Multiplier

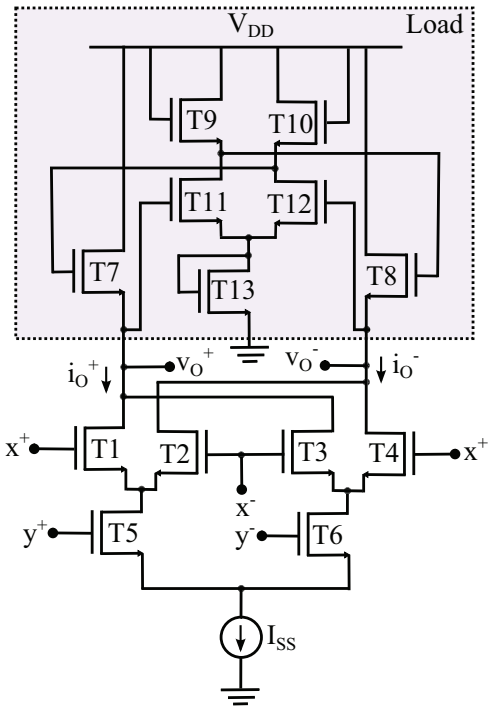


Fig. 6: High gain multiplier

## III. Results

In order to simulate the circuits, a 0.35 $\mu$m CMOS technology was used with a power supply of 3.3 V. The bulk was connected to the source terminal to mitigate the body effect, given that the substrate is an insulator in TFT technologies.

### A. Amplifiers

Transistors dimensions and passive-elements values utilized in all the amplifier topologies are listed in Table. I. When all the amplifiers (Amp1, Amp2 and Amp3) are simulated for the same input bias conditions their frequency response is shown

in Fig. 7. From this ac response, it can be noticed that the Amp1 and Amp3 are capable of amplifying dc, whereas Amp2 is not. Amp1 bandwidth is higher than the other topologies but the gain is the lowest. Whereas, Amp2 and Amp3 promises more gain than Amp1 at the cost of bandwidth. Among all circuits, Amp3 has poorer bandwidth because of extra delay states involved in the feedback network. Table. II shows the power consumption for the different amplifiers. From these results, it can be noticed that Amp1 and Amp2 have the same power consumption. On the other hand, Amp3 draws more power for a gain equal to Amp2.

TABLE I: Circuit components information

| Circuit | Transistors | Capacitors |
|---|---|---|
| Amp1 | T1,T2 : W = 100 $\mu$m, L =20 $\mu$m | - |
| Amp2 | T1,T2 : W = 100 $\mu$m, L =20 $\mu$m<br>T3 : W = 10 $\mu$m, L =10 $\mu$m | C = 95 pf |
| Amp3 | T1,T2 : W = 100 $\mu$m, L =20 $\mu$m<br>T3,T5 : W = 99.9 $\mu$m, L =10 $\mu$m<br>T4,T6 : W =100 $\mu$m, L =10 $\mu$m | - |

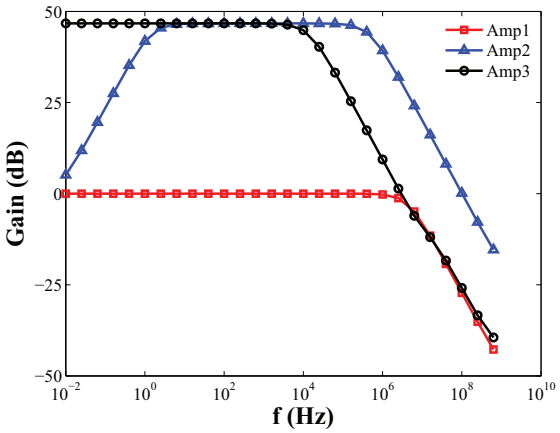


Fig. 7: Amplifiers frequency response

TABLE II: Comparison of power consumption

| Circuit | Power Consumption (mW) |
|---|---|
| Amp1 | 0.109 |
| Amp2 | 0.109 |
| Amp3 | 0.586 |

Fig.8 shows the gain variation with respect to C and T3 dimensions (the width is equal to the length). It can be observed that, for fixed T3 dimensions, high values of C promises more gain as the feedback factor becomes almost close to unity. On the other hand, for fixed value of C, increasing the dimensions of T3 reduces the gain because of its higher capacitance. Consequently, to obtain high gain, T3 dimensions should be as low as possible and C value should be much higher than the intrinsic capacitance of transistors. With larger C values, the low-cutoff frequency can also be reduced so that low frequency signals can be amplified.

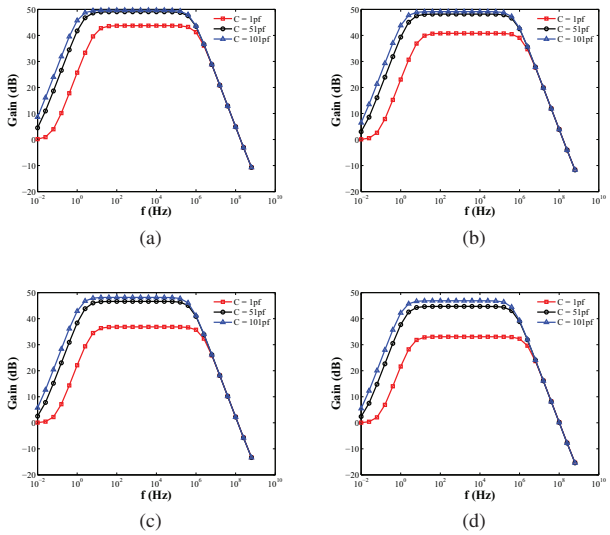


Fig. 8: Impact of C value and T3 dimensions on Amp2 gain (a) W = 1 $\mu$m (b) W = 4 $\mu$m (c) W = 7 $\mu$m (d) W = 10 $\mu$m

Bandwidth dependence on C and T3 dimensions are shown in Fig. 9. This shows that the higher value of C reduces bandwidth in a non-linear way, whereas an increase in T3 dimensions reduces bandwidth almost in a linear manner.

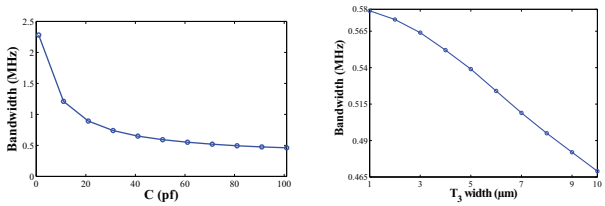


Fig. 9: Amp2 bandwidth variation with respect to: (a) C value (b) T3 dimensions

Amp3 gain and bandwidth variation with respect to the feedback circuit driver transistors (T3 and T5) widths are shown in Fig. 10 and Fig. 11 respectively, when the remaining transistors dimensions are fixed. From these results, it can be noticed that the increase in the T3 and T5 widths are increasing gain but consequently reducing bandwidth.

### *B. Multipliers*

Transistors dimensions used with the multipliers (Mul1 and MuL2), their power consumption and bandwidth are shown in Table. III. Linearity response of the both multipliers and the expected behavior is shown in Fig. 12. It shows that Mul2 is more non-linear compared to Mul1.

For both the multipliers, the following stimulus is applied, in which, one of the input is connected to the signal and other

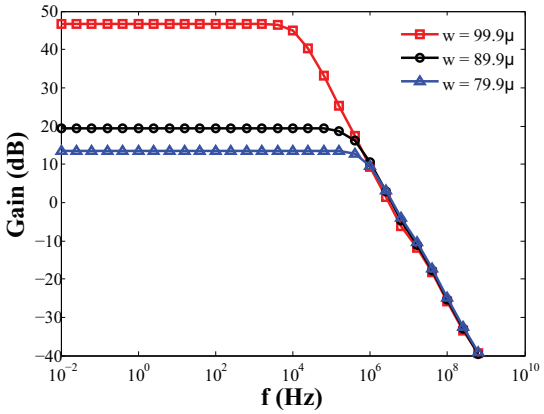


Fig. 10: Amp3 gain variation with T3 and T5 widths

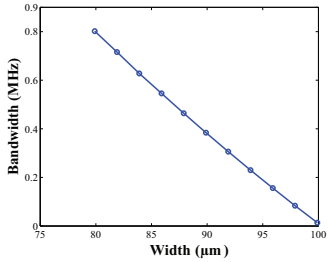


Fig. 11: Amp3 bandwidth variation with T3 and T5 widths

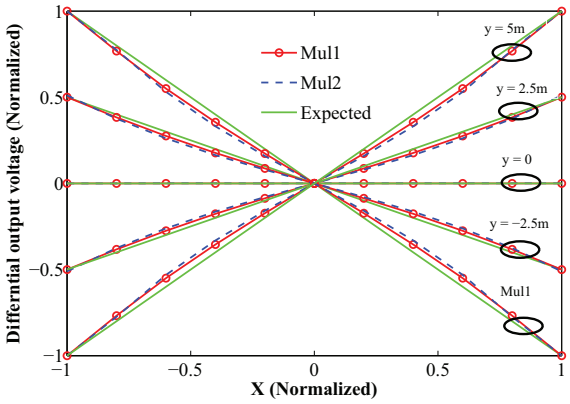


Fig. 12: Mul1 and Mul2 linearity response

to the small dc voltage.

$$x = 1.5 \pm A\sin(\omega_1 t) \quad (9)$$
$$y = 0.7 \pm 0.1$$

The corresponding frequency response of the multipliers are shown in Fig. 13. The proposed multiplier (Mul2) promises higher gain (but consequently lower bandwidth) when compared with the conventional multiplier with diode connected load, due to a much higher equivalent load.

TABLE III: Comparison of power consumption

| Circuit | Transistor dimensions | Power Consumption (mW) | Bandwidth |
|---|---|---|---|
| Mul1 | T1 - T4 : W = 100 $\mu$m, L = 10 $\mu$m<br>T5, T6 and diode connected loads : W = 200 $\mu$m, L = 10 $\mu$m | 0.33 | 10.34 MHz |
| Mul2 | T1 - T4, T9, T10 : W = 100 $\mu$m, L = 10 $\mu$m<br>T5 - T8, T13 : W = 200 $\mu$m, L = 10 $\mu$m<br>T11,T12: W = 99.5 $\mu$m, L = 10 $\mu$m | 0.4 | 27.23 KHz |

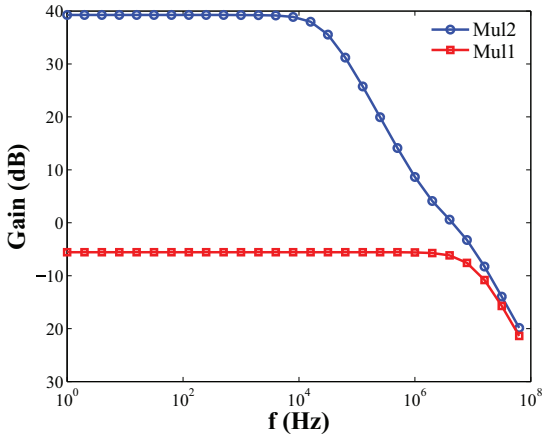


Fig. 13: Mul1 and Mul2 frequency response

## IV. Conclusions

This paper described high-gain amplifier topologies and high-gain multiplier with n-type enhancement transistors. These circuits were simulated with a 0.35$\mu$m technology. During circuit simulations body effect was avoided and also dimensions of the transistors were made large to avoid short channel effects. Hence, these circuits can be directly realized by the transparent technologies that lack a complementary type transistor. Simulation results show that, Amp3 is capable of amplifying dc signals at the cost of bandwidth and higher power consumption when compared to Amp2. Basing on the application requirements either, Amp1 or Amp2 topology can be selected to obtain high gain. To enhance gain even further, cascoding techniques can also be used along with these circuits. A high-gain multiplier also demonstrated using positive feedback concept.

## Appendix

The bandwidth (dominant pole) of Amp3 is calculated using the time constant method. As a first step, the circuit is analyzed without considering feedback. The intrinsic elements of the transistors in the circuit that are contributing to the frequency response are shown in Fig.14. In this circuit, the capacitors $c_{gd2}$, $c_{gd4}$ and $c_{gd6}$ are short-circuited. Fig. 15 shows the simplified equivalent.

The capacitors and resistors in Fig. 15, in terms of the

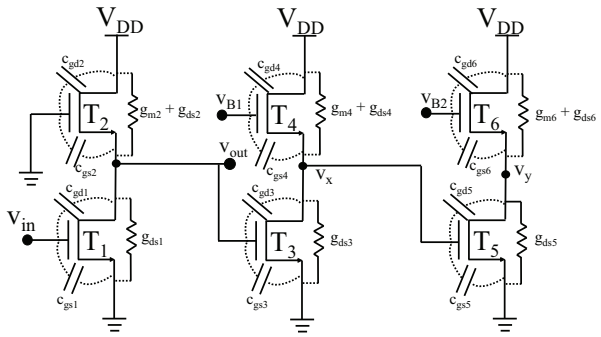


Fig. 14: Amp3 frequency analysis without feedback

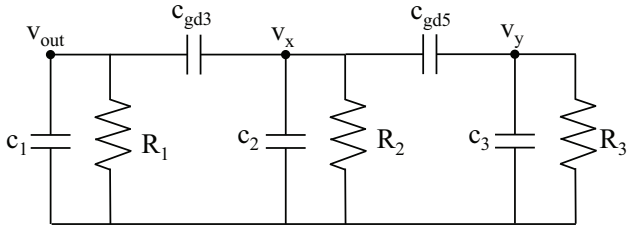


Fig. 15: Passive elements contibuting the frequency response

intrinsic parameters of the transistors are shown below.

$$\begin{aligned} c_1 &= c_{gd1} + c_{gs3} + c_{gs2} \\ c_2 &= c_{gs4} + c_{gs5} \\ c_3 &= c_{gs6} \\ R_1 &= \frac{1}{g_{m2} + g_{ds2} + g_{ds1}} \\ R_2 &= \frac{1}{g_{m4} + g_{ds4} + g_{ds3}} \\ R_3 &= \frac{1}{g_{m6} + g_{ds6} + g_{ds5}} \end{aligned} \tag{10}$$

Individual time constants due to each capacitor are given by,

$$\begin{aligned} \tau_1 &= c_1 R_1; \quad \text{When } c_1 \text{ is active,} \\ \tau_2 &= c_{gd3}(R_1 + R_2); \quad \text{When } c_{gd3} \text{ is active,} \\ \tau_3 &= c_2 R_2; \quad \text{When } c_2 \text{ is active,} \\ \tau_4 &= c_{gd5}(R_2 + R_3); \quad \text{When } c_{gd5} \text{ is active,} \\ \tau_5 &= c_3 R_3; \quad \text{When } c_3 \text{ is active} \end{aligned} \tag{11}$$

$$\begin{aligned} \tau &= \tau_1 + \tau_2 + \tau_3 + \tau_4 + \tau_5 \\ \omega_o &= \frac{1}{\tau} \end{aligned} \tag{12}$$

Then the bandwidth of the Amp3 with feedback is given by,

$$\begin{aligned} \omega_f &= \omega_o(1 - A_f.A_2) \\ A_2 &= \frac{g_{m2}}{g_{m2} + g_{ds2}} \end{aligned} \tag{13}$$

where $A_f$ is the feedback circuit gain and $A_2$ is the source follower (T2) gain in Fig. 3(b).

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