High-gain Amplifier with n-type Transistors

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***Abstract*—A high-gain amplifier topology, with all single n-type enhancement transistors, is proposed in this paper. This type of circuits are essential in transparent TFT technologies, such as GIZO and ZnO that lack complementary type transistor. All circuits were simulated using BSIM3V3 model of a 0.35 μm CMOS technology, due to the absence of a complete electrical model for the TFTs. Results reveal that the proposed circuit promise more gain, lower power consumption and higher bandwidth than the existing solutions under identical bias conditions.**

I. Introduction

In recent years, transparent thin-film transistor (TFT) technologies, such as GIZO [1] and ZnO [2], are captivating a great deal of attention, mainly because these devices can effectively be fabricated at room-temperature. Many sensors with GIZO [3] and ZnO [4] materials have been reported. Designing integrated analog-signal conditioning/processing circuits with the same materials will benefit cost-effectiveness by eliminating interfacing between sensors and reading circuits. One of the main challenges involved in designing analog or mixed signal circuits with these technologies is the lack of a stable complementary (p-type) device, confining the circuit design to only n-type devices.

High-gain amplifier stages are very important blocks to realize operational amplifiers and other signal conditioning circuits. For the current scenario, when a simple common source amplifier is considered, an n-type depletion transistor (whose gate is connected to source) can be used as load to realize high gain. However, depletion technology needs at least one more mask than the enhancement counterpart. Thus, enhancement technology results in more cost-effective solutions, if it is possible to overcome the design challenges. In literature some solutions have been suggested to obtain high gain only with enhancement n-type transistors using positive feedback. A high-gain differential amplifier is proposed in [5] using NMOS transistors. A similar procedure was successfully realized with a-Si:H TFTs in [6], and with single-ended configuration in [7]. This work starts with the conventional bootstrap inverter [8] for analog operation, and then, using the same concept, a novel circuit is proposed to further enhance the gain without compromising power consumption. The proposed circuit exhibit higher bandwidth and lower power consumption when compared to the solution suggested in literature [6] and [7].

II. Amplifier Topologies

The high-gain amplifier, employing successive inverting stages for positive feedback, is shown in Fig. 1 (a) (Amp1). If the feedback gain (A_f) is one, for signal the gate will be short-circuited to the source while keeping transistor T2 in saturation, actually, for proper operation all transistors have to remain in saturation. This setup acts as a high-load impedance. In order to grant a stable operation, always maintain $A_f \leq 1$. Since more delay stages are involved in the feedback circuit, this configuration has limitations on the frequency response. The dimensions of the transistors in the feedback network shows impact on the overall amplifier gain. Alternatively, Fig. 1 (b) (Amp2) shows a bootstrap inverter. When used as an analog amplifier, by means of the capacitor C, the output signal is fed back to the gate of the transistor T2, short-circuiting gate and source for signal. T3 is used to impose bias voltage at T2 gate and T3 remains in cutoff. One should note that the value of C and the dimensions of T3 have influence on the gain.

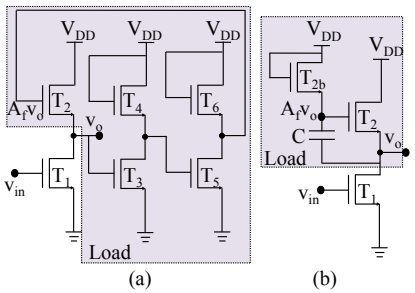

Fig. 1. High gain topology (a) Positive feedback using delay stages [6], [7] (Amp1) (b) NMOS bootstrap inverter to obtain high gain [8] (Amp2)

For both amplifiers shown in Fig. 1, the load impedance is given by (assuming all transistors in saturation, and with the same g_m and g_{ds})

$$R_L = \frac{1}{g_m(1 - A_f) + g_{ds}} \tag{1}$$

The proposed circuit is shown in Fig. 2 (a) (Amp3). It is a double bootstrapped amplifier with high-output impedance. The actual load being maximized is that of T2 that results in the following value seen by T1:

$$R_L \approx \frac{1}{g_m(1 - A_f) + \frac{2(1-A_f)g_m + g_{ds}}{g_m} g_{ds}} \tag{2}$$

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This load is much higher than (1), which reflects in an increased gain. The intrinsic gain of the input transistor can in fact be achieved when the capacitance in the circuit C is significantly higher than the parasitic capacitances of the transistors. In order to increase the gain further, cascoding technique can be employed as shown in Fig. 2 (b) (Amp4).

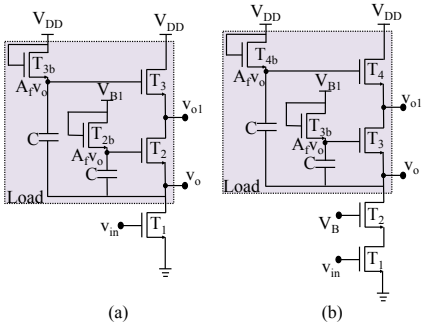

Fig. 2. (a) Proposed high gain amplifier topology (Amp3) (b) With cascoding technique to enhance gain further (Amp4)

III. Results

All the amplifiers are simulated with the BSIM3V3 models in a 0.35 μm technology under identical bias conditions. The dimensions of the circuit elements are shown in Table. I. For Amp1, it has been made sure that A_f does not exceed

TABLE I. Dimensions of circuit elements

Circuit	Transistors	Capacitor
Amp1	T1, T2 : W/L 100/10 μm; T3 - T6 : W/L 5/5 μm	-
Amp2	T1, T2 : W/L 100/10 μm; T_{2b} : W/L 5/5 μm	6.5 pf
Amp3	T1 - T3 : W/L 100/10 μm; T_{2b}, T_{3b} : W/L 5/5 μm	6.5 pf
Amp4	T1 - T4 : W/L 100/10 μm; T_{2b}, T_{3b} : W/L 5/5 μm	6.5 pf

one by means of the bias voltages. Frequency response of all amplifiers are shown in Fig. 3 with same A_f. This shows that the Amp2 and Amp3 have higher gain than that of Amp1 and Amp2. All the amplifiers load resistance, gain, bandwidth and

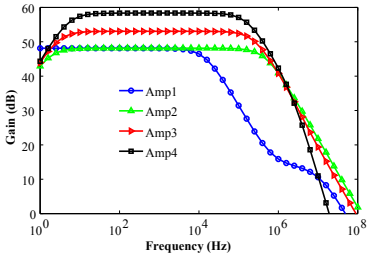

Fig. 3. Ferquency response of the all amplifiers under indentical bias vonditions

power consumptions are reported in Table. II. It shows that the Amp2, Amp3 and Amp4 have less power consumption and higher bandwidth compared to Amp1. Amp3 and Amp4 gain can be increased significantly by employing higher values of capacitance as shown in Fig. 4.

IV. Conclusion

A high-gain amplifier topology using only n-type transistors is proposed for TFT technologies, which lack complementary type transistor. The circuits in this work are more stable

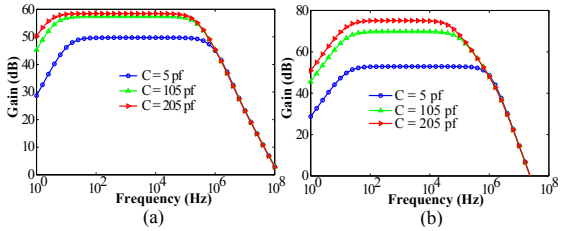

Fig. 4. Gain variation with respect to the capacitance value (a) Amp3 (b) Amp4

TABLE II. Performance comparison

Circuit	Load (when Af = 1)	Gain	Bandwidth (Hz)	Power consumption (mw)
Amp1	$\approx r_{ds}$	$\approx 0.5 g_m r_{ds}$	73.73 K	0.225
Amp2	$\approx r_{ds}$	$\approx 0.5 g_m r_{ds}$	3.21 M	0.1727
Amp3	$\approx g_m r_{ds}^2$	$\approx g_m r_{ds}$	2.936 M	0.1727
Amp4	$\approx g_m r_{ds}^2$	$\approx 0.5 (g_m r_{ds})^2$	2.672 M	0.1727

and have shown higher bandwidth, lower power consumption when compared to the circuit with positive feedback using delay stages. However, it does not amplify dc, but one can program the lower cutt-off frequency to values close to zero.

Acknowledgment

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