# A Low-Power Multi-Tanh OTA with Very Low Harmonic Distortion

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***Abstract*—This paper presents a wide input range, low-power operational transconductance amplifier (OTA) in weak inversion. The OTA is implemented with tanh-triplets differential pairs, degenerated by a composite configuration to augment the input linear range, thus reducing further the harmonic distortion. Using MATLAB, the mismatch factor (A) of a typical multi-tanh triplet has been optimised for minimum harmonic distortion. The OTA is designed in UMC 0.13um CMOS technology with 1.2V supply. Simulations show that the input range can be extended to 300 mV, while keeping the HD3 below -80 dB. The average power consumption is 13nW, with an open loop-gain of 76 dB and a unity gain frequency of 250 Hz. The low harmonic distortion OTA can find potential applications in low-power and long time constant filters.**

***Index Terms*—Ultra low power OTA, low harmonic distortion, high linearity.**

## I. Introduction

The operational transconductance amplifier (OTA) is one of the most widely-used building blocks in analog signal processing applications. For biomedical systems, in particular, OTAs are often involved in circuits that inherently need to be very limited in frequency, involving very large time constants. Transconductance values in the range of tens of p℧ to a few tens of n℧ are normal in this type of applications [1].

OTAs are accurately utilized in active circuits to mimic passive elements. This is a common practice in Gm-C filter design. In such cases, the linearity of the OTA characteristic (I/V) becomes critical. However, a variety of techniques are available for linearity improvement, such as: (1) *source degeneration* [1], [2], (2) *cancellation of nonlinear terms* [3] with auxiliary circuit blocks (leading to more power consumption), (3) *triode based transconductor* where the input differential pair is biased in triode region [4], or (4) *voltage attenuation*. In the last a transconductance attenuator is needed at the input stage, either a bulk-driven differential pair [5], [6], an OTA-based resistive network [7], or a modular technique using ordinary linear differential pairs [8]. The major problem associated with gate-driven OTAs in weak inversion resides in the input linear range, which is usually very limited. Keeping a total harmonic distortion (THD) in values below -40 dB demands an input range no higher than a few tens of millivolt [6]. As referred earlier, bulk-driven topologies can successfully be applied to increase the OTA linearity [6], [9]. However, they present some major drawbacks such as lower gain bandwidth (GBW) and higher input referred noise. Also, for an n-well process, bulk driven MOSFETs are confined to p-type devices.

In this paper, a low power low-harmonic distortion gate-driven OTA is proposed by combining both the multi-tanh technique and emitter degeneration. This particular configuration is what Gilbert called "Hybrid Triplet" [2]. Results show that both low THD and low transconductance can be achieved with little cost on power consumption. The rest of this paper is organized as follows. In section II, a typical non-degenerated multi-tanh triplet in weak inversion is described and an equation for 3rd harmonic distortion (HD3) is derived. In section III, the proposed circuit is discussed, followed by simulation results in section IV. Finally, conclusions are drawn in section V.

## II. MOS Multi-Tanh Triplet in weak inversion

In weak inversion, the majority carriers are repelled away from the channel region; however, the density of minority carriers is still small. Typically, the weak inversion current lies roughly in the range of $10^{-9}$ to $10^{-7}$ ampere [10], [11]. When a MOS transistor is operating in this region, the current mechanism is essentially determined by diffusion and the control function becomes exponential, as represented in (1) [11],

$$I_{DS} = I_M(\frac{W}{L})exp(\frac{V_{GS}-V_M}{n\phi_t})[1-exp\frac{-V_{DS}}{\phi_t}] \quad (1)$$

$I_M$ is the characteristic current, which is in the order of $10^{-15}$ to $10^{-12}$ amperes; $V_M$ is the upper limit of weak inversion in terms of $V_{GS}$ (coincides with the threshold voltage), for a fixed source-bulk voltage ($V_{SB}$); $\phi_t = kT/q$; and $n$ is the slope factor that represents the effect of the capacitive division: $\frac{C_{ox}+C_D}{C_{ox}}$, formed by the oxide capacitance $C_{ox}$ and the depletion capacitance $C_D$ [12]. Note that the drain-source current in (1) will be independent of $V_{DS}$ when $V_{DS} \geq 3\phi_t$, so that with less than 5% error the last exponential term becomes negligible compared to 1 and can be dropped [11]. Furthermore, by combining the dependencies on $I_M$ and $V_M$, simply we have:

$$I_{DS} = I_{Do}(\frac{W}{L})exp(V_{GS}/(n\phi_t)) \quad (2)$$

wherein $I_{Do} = I_M exp(\frac{-V_M}{n\phi_t})$. Using equation (2) and the fact that $tanh(x) = (e^{2x}-1)/(e^{2x}+1)$, it can easily be

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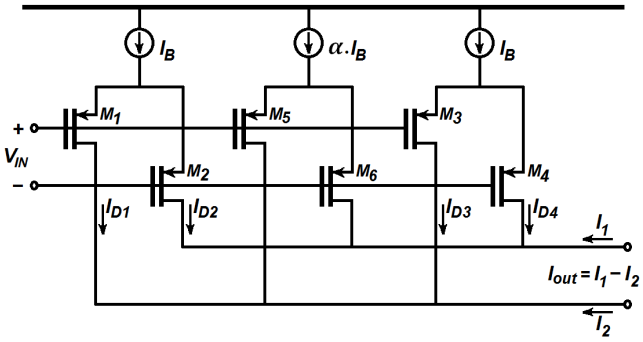


Fig. 1. A simple PMOS pair multi-tanh triplet

demonstrated that equation (3) represents the transfer function of a MOS differential pair operating in weak inversion, with tail current $I_B$,

$$I_o = I_{D1} - I_{D2} = I_B tanh(V_{IN}/(2n\phi_t)) \tag{3}$$

where $I_o$ is the output differential current, $I_{D1,2}$ are drain currents and $V_{IN}$ is the input voltage. Equation (3) is valid for a differential pair circuit when both MOS transistors are matched. If the aspect ratio of one of the transistors is $\boldsymbol{A}$ times the other, an equivalent offset voltage $V_{OS} = \phi_t ln(A)$ will develop, resulting in a shift of the transfer function [2]. Now, consider three differential pairs in parallel, the so-called multi-tanh triplet, as Fig. 1 illustrates, with ratio of transistor sizes defined by (4):

$$(\frac{W}{L})_{M_{1,4}}/(\frac{W}{L})_{M_{2,3}} = A \tag{4}$$

The differential pairs represented by the sets M1 – M2, and M3 – M4 show a voltage offset with the same absolute value, but in opposite directions of the transfer characteristic. The differential pair in the middle, M5 – M6, is added to smooth the transconductance in the linear range, reducing its fluctuations along the full extent of operation. In fact, M5 and M6 must be matched with M2 and M4 and fed by a separate current source with an attenuation factor ($\alpha$) as illustrated in Fig. 1. Thus, the pair in the middle does not show a voltage offset, and exhibits a lower maximum current than the other two neighboring pairs. Finally equations (5), (6) and (7) can be obtained,

$$I_{D1} - I_{D2} = I_B tanh(\frac{V_{IN} + V_{OS}}{2n\phi_t}) \tag{5}$$

$$I_{D5} - I_{D6} = \alpha.I_B tanh(\frac{V_{IN}}{2n\phi_t}) \tag{6}$$

$$I_{D3} - I_{D4} = I_B tanh(\frac{V_{IN} - V_{OS}}{2n\phi_t}) \tag{7}$$

where $I_B$ (and $\alpha.I_B$) is the tail current of each differential pair. Adding up equations (5), (6) and (7) results in the total output current ($I_{out}$), represented by equation (8); it describes output current in terms of differential input voltage ($V_{IN}$) for a typical non-degenerated MOS-based multi-tanh triplet.

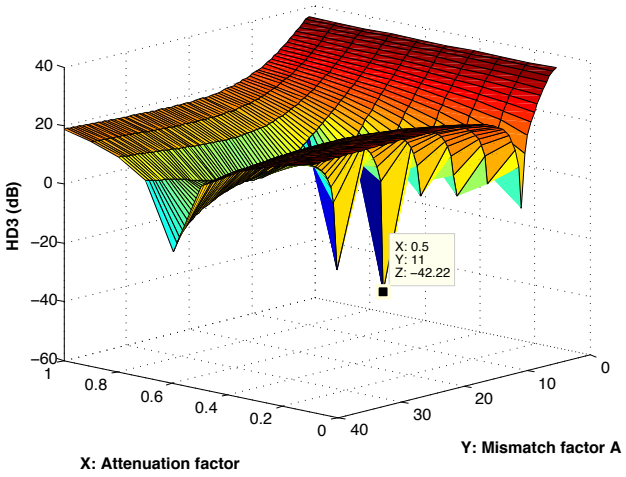


Fig. 2. Optimum HD3 for different offset voltage and attenuation factor in a tanh triplet

$$I_{out} = I_B[tanh(\frac{V_{IN} + V_{OS}}{2n\phi_t}) + \alpha.tanh(\frac{V_{IN}}{2n\phi_t}) + tanh(\frac{V_{IN} - V_{OS}}{2n\phi_t})] \tag{8}$$

The ratio between the first and the third coefficient in the Taylor series expansion of $I_{out}$, around the central point, gives the 3rd Harmonic Distortion (HD3) component:

$$HD3 = (\frac{-1}{12(2+\alpha)n^2{\phi_t}^2})[2 + \alpha - 8tanh(\frac{V_{OS}}{2n\phi_t})^2 + 6tanh(\frac{V_{OS}}{2n\phi_t})^4]. \tag{9}$$

In this equation HD3 is a function of $\alpha$ and $V_{OS}$. For a non-degenerated multi-tanh triplet, the smallest possible 3rd harmonic distortion is around -42 dB as shown in Fig. 2. Defining a slope factor of $n = 1.3$, it occurs for an attenuation coefficient $\alpha = 0.5$ and for a mismatch factor of $A = 11$. Consequently, to achieve the smallest HD3 the optimum mismatch factor should be 11, which remains the same if the multi-tanh triplet (all pairs) is source degenerated.

## III. Proposed OTA Design

Linearity is a key factor in every circuit and system. The improvement of that feature ameliorates the amplifier characteristics by relieving the impairments that cause harmonic distortion. In the proposed OTA the multi-tanh triplet – presented in the previous section – has been used to enhance the linearity of the circuit in order to suppress the harmonic distortion. For the multi-tanh OTA, a trade-off between distortion and linear input range needs to be considered. A smaller input range or equivalently less mismatch factor ($\boldsymbol{A}$ in equation (4)) in multi-tanh differential pairs leads to less distortion. On the other hand, increasing the mismatch factor means more input range but more distortion as well. To better tackle this trade-off, one

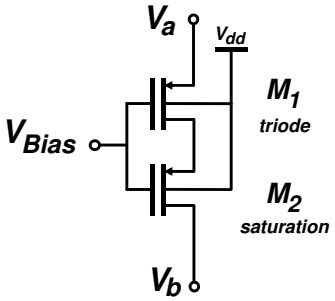


Fig. 3. Composite transistor

either use more mismatched differential pairs, or add source degeneration to increase the linearity of the OTA input stage. The most commonly used topology is the diode-connected MOSFET [2]. However, to further increase the linearity, this work proposes instead a source degeneration technique with composite transistors [13] shown in Fig. 3. Figure 4 presents the final OTA circuit.

Basically, in a composite structure if M2 is *m*-times wider than M1 (i.e., $m = (\frac{W}{L})_2/(\frac{W}{L})_1$ in Fig. 3) the set can be treated as long channel transistor [14]. It is a form of building equivalent bigger sized transistors from arrangements, in series and/or in parallel, of unit size MOSFETs, which improves matching and channel-length modulation [13]. In the case of *m*=1, M1 is set to triode, while M2 will be driven into saturation, as long as enough headroom is given. If $m$ becomes large enough, eventually M1 will also reach saturation. However, taken the value of $V_{DS}$ for M1, as defined by (10) in weak inversion [6], a large $m$ is needed to remove it from triode. So, in practical terms typically M1 remains always in triode.

$$V_{DS1} = \phi_t \cdot \ln\left(1 + \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1}\right) \tag{10}$$

It should be noted that for high frequency applications $m$ should be kept small in order to reduce $C_{GS}$, however a larger ratio minimizes the noise seen at the drain of M2 [14]. Considering both constraints, if low-frequency operation is considered, the intrinsic capacitors of MOSFETs are not too critical, thus a higher $m$ can be employed for noise minimization. This is particularly important for biomedical applications.

Figure 5 shows a comparison of the OTA in Fig. 4 in its form with the composite configuration or with diode-connected degeneration. It becomes apparent that the composite structure not only boosts the linear input range, but also shows that a lower distortion can be achieved (less fluctuation on $G_m$ in Fig. 5). In fact, as referred above, the stack of M1 and M2 effectively mitigates channel length modulation [15], even if minimum lengths are used for both transistors, which increases the equivalent resistance seen at the drain of M2. This larger resistor is responsible for the wider input range

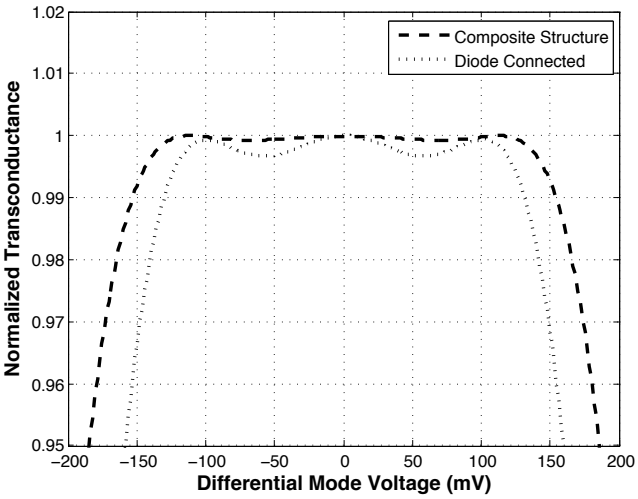


Fig. 5. Linearity comparison between diode-connected MOS (dotted line) and self-cascode (dashed line) for degeneration purposes

For the current mirror stage, the above-mentioned composite structure is also used as a series-parallel current mirror with a copy factor of 1 (see Fig. 4). Given the known improvement that a composite structure brings in terms of channel length modulation, a high impedance is expected at the output of the OTA, in the order of $(m/2)\cdot r_o$ [14]. Furthermore, considering that M1 in Fig. 3 is biased in triode region and M2 operates in saturation, the output headroom becomes typically close to $V_{DSsat}$ of those two transistors directly connected to the output of the OTA (Fig. 4).

TABLE I
PERFORMANCE SUMMERY OF THE PROPOSED OTA AND A COMPARISON TO SIMULATION RESULTS OF A RECENTLY PUBLISHED PAPER

| Specification | Ferreira [6] | This Work |
|---|---|---|
| Technology | IBM 130 nm | UMC 130nm |
| Power supply | 500 mV | 1.2 V |
| Power Consumption | 25 nW | 13 nW |
| THD and HD3 | $\leq -60dB$ | $\leq -80dB$ |
| Input referred thermal noise | 170 $\mu V_{rms}$ | 182 $\mu V_{rms}$ |
| Transconductance | 24 nS | 37 nS |
| Linear Input Range ($\leq -60dB$) | 300 mV | 340 mV |
| Signal-to-Noise Ratio | 62 dB | 62.4 dB |
| Unity Gain Frequency | 124 Hz | 250 Hz |
| Open Loop Gain | 46 dB | 76 dB |
| Topology | Bulk-driven | Gate-driven |

## IV. SIMULATION RESULTS

The low-power low-distortion OTA was designed in UMC 130nm technology with 1.2V power-supply. With some modifications in transistor sizes, the circuit could also be designed for lower power-supply. However, higher supply voltage provides larger voltage headroom and better signal to noise ratio. The biasing current ($I_B$) was set to 2 nA, which forcibly biases the circuit in weak inversion. The OTA consumes around 13 nW. Simulation shows a linearity of roughly 340 mV, considering a 2% variation in $G_m$. Fig. 6 presents the THD

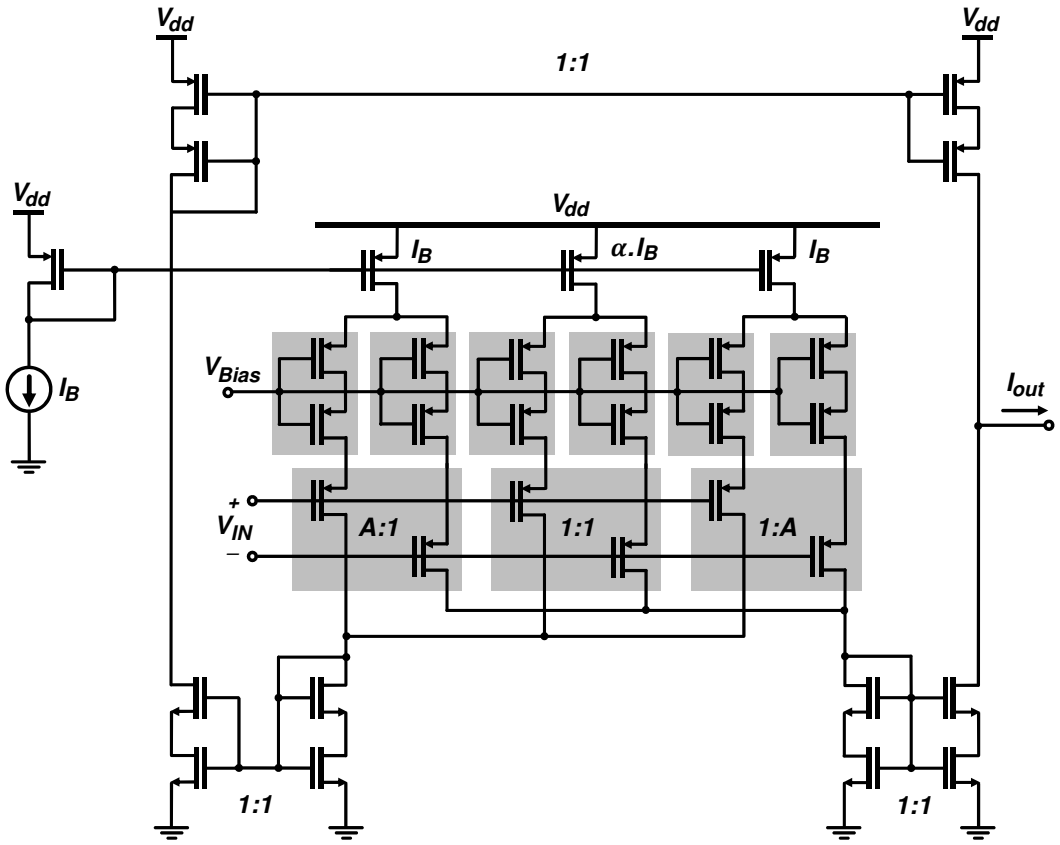


Fig. 4. OTA circuitry

versus the amplitude of the input differential voltage, which is almost always less than -80 dB for a good part of the linear input-range (300 mV out of the 340 mV). The frequency characteristics are extracted with a load capacitor of 15 pF. The open loop-gain is 76 dB with a unity-gain frequency of 250 Hz.

Low frequency circuits are always more prone to noise, specially flicker noise which is dominant at low frequency. The Input referred noise, considered between 0.1 Hz and 100 Hz for comparison purposes with [6], is $182\mu V_{RMS}$, which is relatively high; but the wider input range allows a maximum signal-to-noise ratio of 62.4 dB. All these simulation results are summarized in TABLE I.

## V. Conclusion

In this paper, a low-power low-THD multi-tanh triplet OTA was presented, using a new method to degenerate differential pairs with a composite transistor configuration. Mathematically, it is proved that a multi-tanh triplet shows an almost -40 dB HD3 without source degeneration. With source degeneration, the THD of the OTA is improved to values lower than -80 dB almost in the full input linear-range (300 mV out of the full linear-range, 340 mV). The power consumption of the OTA is found to be around 13 nW. Due to its low THD and power consumption, the proposed OTA is eminently applicable in biomedical implants and sensor nodes in WSNs.

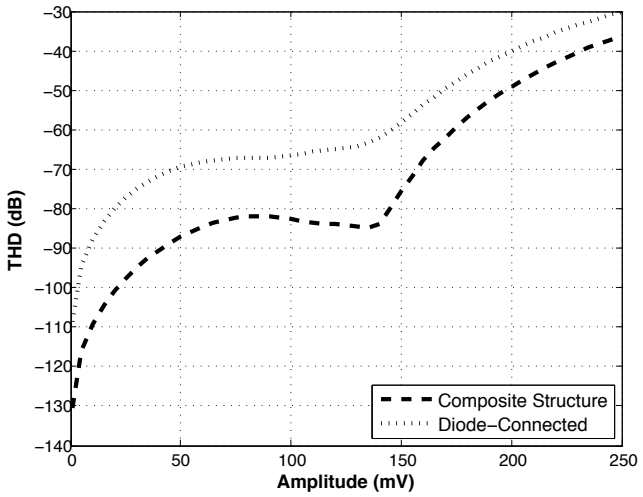


Fig. 6. Total Harmonic Distorsion (THD) for different input voltage amplitude applying a 1 Hz sine wave

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