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Influence of Channel Length Scaling on InGaZnO TFTs Characteristics: Unity Current-Gain Cutoff Frequency, Intrinsic Voltage-Gain, and On-Resistance

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***Abstract*—This paper presents a study concerning the role of channel length scaling on IGZO TFT technology benchmark parameters, which are fabricated at temperatures not exceeding 180 °C. The parameters under investigation are unity current-gain cutoff frequency, intrinsic voltage-gain, and on-resistance of the bottom-gate IGZO TFTs. As the channel length varies from 160 to 3 μm, the measured cutoff frequency increases from 163 kHz to 111.5 MHz, which is a superior value compared to the other competing low-temperature thin-film technologies, such as organic TFTs. On the other hand, for the same transistor dimensions, the measured intrinsic voltage-gain is changing from 165 to 5.3 and the on-resistance is decreasing from 1135.6 to 26.1 kΩ. TFTs with smaller channel length (3 μm) have shown a highly negative turn-on voltage and hump in the subthreshold region, which can be attributed to short channel effects. The results obtained here, together with their interpretation based on device physics, provide crucial information for accurate IC design, enabling an adequate selection of device dimensions to maximize the performance of different circuit building blocks assuring the multifunctionality demanded by system-on-panel concepts.**

***Index Terms*—Intrinsic voltage-gain, unity current-gain cutoff frequency, IGZO TFTs and channel length scaling.**

I. Introduction

INDIUM-GALLIUM-ZINC oxide thin-film transistors (IGZO TFTs) are becoming a reference technology for flexible, ultra-definition or even transparent display backplanes. This arises as a consequence of their high mobility, good stability, large area uniformity and compatibility with low cost/low-temperature processing techniques [1]. More than simple switching elements, IGZO TFTs have been integrated in important building blocks such as amplifiers [2], [3], comparators [4], data converters [5] and driving circuits [6], facilitating their integration in increasingly complex systems. As such, there is a continuous drive to design novel and efficient circuits based on miniaturized devices to enhance speed and integration levels. This will ultimately lead to compact system-on-panel products, where a display is seamlessly integrated with peripheral circuits and even sensors, for increased performance, reliability and functionality.

However, channel length L scaling affects several device parameters such as unity current-gain cutoff frequency f_T, intrinsic voltage-gain A_V, and on-resistance R_{ON}. In addition to the techniques and architectures used for circuit design, these parameters will dictate the circuit performance.

The importance of these parameters is summarized as follows:

f_T : Switching speed is an important parameter in high frequency applications, especially when the circuits are designed for RF systems. Beyond f_T, a transistor cannot show proper functionality and often circuit operating frequency is limited by this value.

A_V : This is the maximum gain that a single transistor can achieve. Even with a single stage amplifier the maximum achievable gain is less than or equal to A_V. As IGZO TFT based amplifiers are important functional blocks for various applications, it is important to know the value of A_V.

R_{ON}: It gives an insight on the device switching performance. Potential applications of TFT switches are in displays, readout circuits and dynamic biasing. This parameter also provides information about the channel noise [7], [8], which generally imposes limitation on the minimum signal level that can be processed. This information is really important in sensor interface electronics.

Based on this it is imperative to study the effect of channel length scaling on these device parameters. In literature, A_V higher than 1000 has been reported for polysilicon source-gated TFTs [9]. In addition, microwave frequency operation was demonstrated for ZnO TFTs [10]. However these devices are not suitable for large area flexible electronics, due to the polycrystalline structure of the semiconductor and high temperature processing. On the other hand, f_T of 64 kHz for

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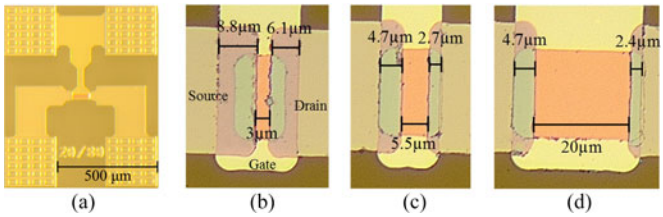

Fig. 1. Micrograph of the fabricated IGZO TFTs. (a) Schematic. (b) Pictures showing the channel length and gate to source/drain overlap.

organic TFTs fabricated with low temperature techniques were reported [11], whose performance is not adequate for moderate high frequency applications. Moreover, most of these reports are focused on single device dimensions. Channel length scaling has been analyzed on ZnO [12] and IGZO TFTs [13] but only regarding their static characterization, whereas the analysis of dynamic behavior is essential for circuit design. To the best of author's knowledge this is the first time that such results are reported for IGZO TFTs with respect to channel length scaling, contributing to define the range of applications that can be envisaged for such technology.

II. TFT Fabrication

Sputtered staggered bottom-gate, top contact TFTs on glass were produced as follows: a 60 nm thick Molybdenum (Mo) gate electrode and a 100 nm thick 7-layer multicomponent oxide (comprising SiO_2 and Ta_2O_5 alternating layers) dielectric [14] were sputtered and patterned by photolithography and dry-etching. A 40 nm thick amorphous IGZO (with 2:1:1 composition in In:Ga:Zn atomic ratio [15]) channel layer was then deposited, also by sputtering. Later, source and drain electrodes were sputtered using 60 nm thick Mo. Semiconductor and source-drain electrodes were patterned by photolithography and lift-off. At the end devices were subjected to rapid thermal annealing at 180 °C for 10 min in air. The fabrication process can be easily adopted to commercial polymeric films. In fact, device scaling trends reported below were seen equally on glass and PEN. Still, in order to extend the L range to the low end of the μm scale, devices on Corning Eagle glass were preferred for this study, as the available lithography process requires further tuning to obtain L $\leq$ 5 μm reliably on flexible PEN substrates. Micrograph of the fabricated TFT and magnifications of the gate to source/drain overlap for different L are presented in Fig. 1. Devices with smaller L (= 3 μm) present a larger gate to source-drain overlap for enhanced process margin.

III. Static Characterization of TFTs

All the device measurements were taken using a semiconductor parameter analyzer (Keithley 4200-SCS) together with a probe station (Janis ST-500) under darkroom conditions at room temperature. The TFTs under study have a constant width W of 20 μm and different L (3, 5, 10, 20, 40, 80 and 160 μm).

Fig. 2 presents the output characteristics of two TFTs with L = 5 and 40 μm. From these plots, it is evident that the TFT with L = 5 μm shows non-saturation behavior, as the channel

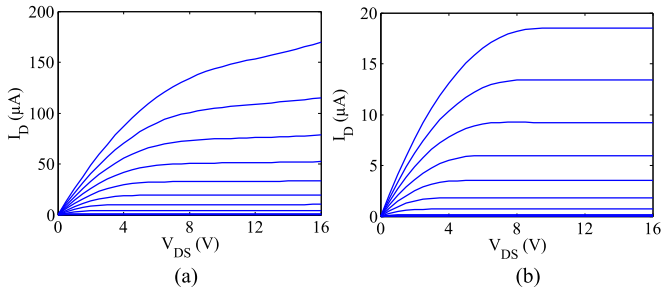

Fig. 2. IGZO TFTs output characteristics for V_{GS} = −2–8 V in steps of 1 V and V_{DS} = 0–16 V in steps of 0.5 V. (a) L = 5 μm. (b) L = 40 μm.

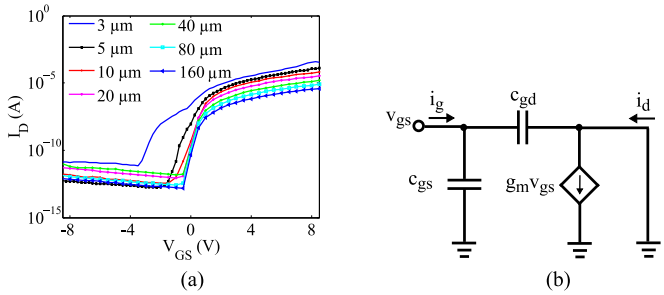

Fig. 3. (a) Transfer characteristics of IGZO TFTs with different L for V_{GS} = −8.5–8.5 V in steps of 0.5 V and V_{DS} = 16 V. (b) TFT small signal model considered for f_T evaluation.

length modulation (CLM) effect is more significant for smaller L, i.e., the reduction of the channel length after pinch-off starts to be significant considering the overall L defined geometrically by the mask layout. On the other hand, long channel device with L = 40 μm shows hard saturation. CLM effect is also responsible for the overestimated saturation mobility (μ_{sat}) extracted from transfer characteristics [see Fig. 3(a)] for L $\leq$ 5 μm, where values of $>$ 18.5 cm^2/V·s are obtained, compared to $\approx$ 13.8 cm^2/V·s calculated for L = 10–160 μm. Transfer characteristics of TFTs with smaller L (3 μm) show a hump in the sub-threshold region and highly negative V_{ON} (= −3.5 V, see also Table I) due to short channel effects (SCEs), mainly because of the drain induced barrier lowering (DIBL) in oxide TFTs [16]. Note that the hump is still observed for measurements repeated after more than seven months of fabrication. These short-channel devices tend to operate in depletion mode and are not a perfect choice for switching and logic circuits.

IV. Benchmark Parameters Measurements

f_T: It is the frequency where the input signal current i_g is the same as the output signal current i_d, when a voltage signal with small amplitude is applied at the gate and a constant dc voltage at the drain electrode. Corresponding TFT small signal model to estimate f_T is shown in Fig. 3(b). When the drain current passing through c_{gd} is neglected, f_T can be mathematically expressed by

$$f_T \approx \frac{g_m}{2\pi c} \tag{1}$$

TABLE I
DEVICE CHARACTERISTICS WITH DIFFERENT CHANNEL LENGTHS

V (μm)	V_{on} (V)	g_m (μS)	g_{ds} (μS)	A_V	c_g (fF)	f_T^1 (MHz)	f_T^2 (MHz)	R_{ON} (kΩ)
160	−0.5	9.5e−1	5.7e−3	166.6	925	1.6e−1	1.6e−1	1135.6
80	−0.5	1.9	1.8e−2	105.5	512	5.9e−1	5.90e−1	516.5
40	−0.5	3.7	5.5e−2	67.2	315	1.9	1.9	283.2
20	−0.5	8.0	1.9e−1	42.1	235	5.4	5.60	137.3
10	−0.9	15.9	1.1	13.6	190	13.4	14.0	73.3
5	−1.5	38.0	4.5	8.6	160	35.8	39.4	39.6
3	−3.5	132.0	25.0	5.3	211	99.5	111.5	26.1

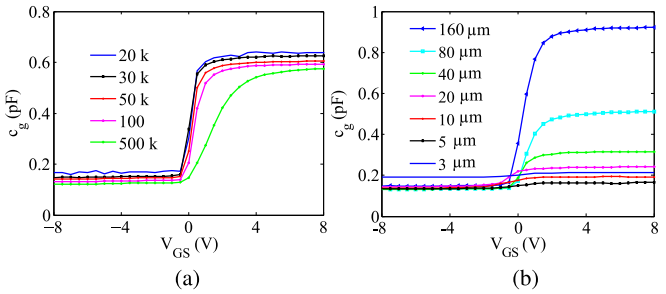

Fig. 4. Total gate capacitance of IGZO TFTs (a) At different frequencies when $V_{DS} = 0$ V, for W $= 20$ μm and L $= 80$ μm. (b) At frequency $= 30$ kHz, $V_{DS} = 16$ V for different L.

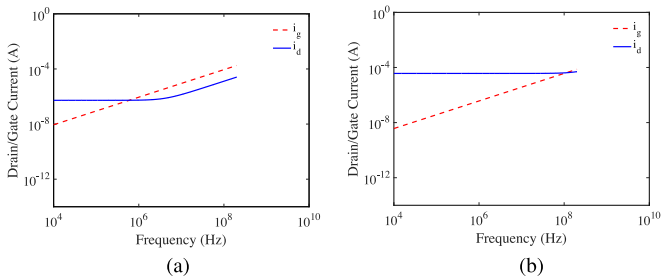

Fig. 5. f_T of IGZO TFTs with different L, determined using i_d and i_g, when a small signal is applied at gate. (a) L $= 80$ μm. (b) L $= 3$ μm.

where g_m is the transconductance and c_g is the total gate capacitance. Measured g_m and c_g at a fixed bias point ($V_{GS} =$ 8 V and $V_{DS} = 16$ V) were used to calculate f_T. In the *C–V* measurements (required to determine c_g), a small signal with 100 mV rms amplitude was superimposed on the dc sweep of gate bias. *C–V* plots at different frequencies are presented in Fig. 4(a), when V_{GS} is swept from −8 to 8 V and $V_{DS} = 0$ V for a TFT with L $= 80$ μm. This plot demonstrates that there is an abrupt increase of total gate capacitance, which is in agreement with the sharp turn on obtained from the *I–V* transfer curve (see Fig. 3(a)). It can be noticed that c_g follows approximately the same trend for the TFT with 80 μm, until a signal frequency $\leq$ 100 KHz. At higher frequencies, however, the inertia of the charge carriers cannot be ignored, which is reflected in the measurements as a smaller total gate capacitance [17]. However, given the relatively small gate to source/drain overlaps used in the present work, we did not notice overlap capacitance variation with respect to frequency until 5 MHz, contrarily to what is typically reported for larger organic TFTs [11]. Later, c_g was measured again for $V_{DS} = 16$ V with an input signal frequency of 30 kHz, which is much smaller than the device cutoff frequencies considered in this study [see Fig. 4(b)]. As the drain is supplied with a constant dc bias voltage, it acts as an ac ground. Therefore measured capacitance represents the total gate capacitance even though the source and drain terminals are at different potentials. Since the channel gets pinched off at higher values of V_{DS}, the measured c_g at $V_{DS} = 16$ V is relatively smaller compared to c_g at $V_{DS} = 0$ V. It can also be noticed from Fig. 4(b) that c_g is higher for the TFT with L $= 3$ μm compared to L $= 5$ and 10 μm, which is well explained by the larger gate to source/drain overlap as shown in Fig. 1(b). Measured c_g values for different L are presented in Table I. It is clear that c_g does not scale linearly with L. This is expected given that as L decreases the gate/dielectric/semiconductor/source-drain overlap area remains constant, as imposed by the mask design. For L $= 3$ μm, c_g even increases, owing to the existent gate to source-drain overlap to enhance process margin, as explained in Fig. 1(b). Table I also presents the estimated f_T (f_{T1}) from (1), varying almost three orders of magnitude for the range of L used in this work. These values are also calculated by considering the current passing through c_{gd} from the TFT small signal model shown in Fig. 3(b). The modulation current at input (i_g) and output (i_d) due to the input signal are given by

$$i_g = 2\pi f c_g v_{gs} \qquad (2)$$
$$i_d = \left[\sqrt{g_m^2 + (2\pi f c_{gd})^2}\right] v_{gs}.$$

Above f_T, i_d increases with f, as shown particularly in Fig. 5(a). Current passing through the capacitance between the gate and the drain electrodes causes this. On the other hand, i_g is proportional to f as per (2). Estimated i_g and i_d from (2) are shown in Fig. 5 for two TFTs with L $= 80$ and 3 μm. Resulting f_T (where i_g and i_d intersect) is presented in Table I as f_{T2} (assuming c_{gd} as half of the total overlap capacitance) and it can be noticed that these values are in good agreement with f_{T1} for long channel devices. For smaller L the minor differences between f_{T1} and f_{T2} are due to the noticeable current through c_{gd} because of comparable overlap dimensions to the actual channel lengths. Fig. 6(a) shows f_{T1} variation with respect to L, revealing that close to 100 MHz operation can be achieved with microscale IGZO TFTs fabricated at low temperature.

A_V : Intrinsic gain of the device is expressed by $\frac{g_m}{g_{ds}}$, where g_{ds} is the output conductance. Measured g_m and g_{ds} in saturation (at $V_{GS} = 8$ V and $V_{DS} = 16$ V) are presented in Table I. For the

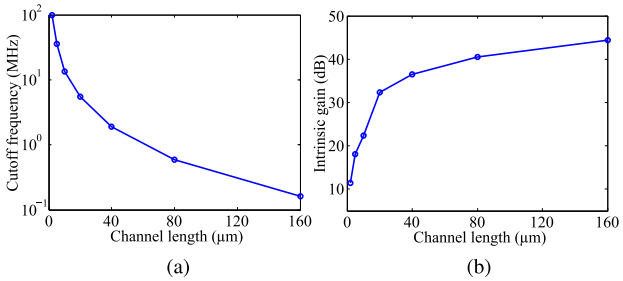

Fig. 6. (a) Cutoff frequency in MHz. (b) Intrinsic gain in dB.

same W, g_m scales with respect to L as

$$g_m = \mu c_{\text{ox}} \frac{W}{L}(V_{\text{GS}} - V_{\text{TH}}) \tag{3}$$

where c_{ox} and V_{TH} are the gate oxide capacitance and threshold voltage, respectively. Both g_m and g_{ds} scale quite well with respect to L, at least for L $\geq$ 5 μm. For smaller L, a large increase is verified in these parameters (mostly in g_{ds}), due to significant CLM effect, as evident from Fig. 2. Therefore, devices with smaller L result in poor A_V [see Fig. 6(b)]. From Table I it can be noticed that there is a tradeoff between the intrinsic parameters A_V and f_T. As L is getting shorter, though high frequency of operation is achieved, A_V value decreases as explained above. For analog circuits operating at moderate frequency it is advisable to use a device with a channel length larger than the critical value where SCEs come into picture.

R_{ON}: Devices are biased in the linear region to determine R_{ON} ($= V_{\text{DS}}/I_d$) from the measured I_d. Its value with respect to different L is given in Table I at a bias condition $V_{\text{GS}} = 8$ V and $V_{\text{DS}} = 0.1$ V. It can be seen that R_{ON} scales linearly with L, meaning that contact resistance effects are not significant even for the lower L studied here. Though smaller channel length devices show less R_{ON} they are not perfect candidates for switches as they operate in depletion mode. Hence, despite the devices shown here seem to be excellent candidates for low-temperature MHz range analog signal processing circuits, their application as switches at such frequencies requires further optimization to achieve $V_{\text{ON}} \geq 0$ V without significant degradation of μ_{sat}. This can be achieved, for instance, with tuning of IGZO composition [18].

V. Conclusion

Effects of channel length scaling (3 to 160 μm) on f_T, A_V and R_{ON} are reported for sputtered IGZO TFTs fabricated at a maximum temperature of 180 °C. TFTs with smaller L exhibit operation frequencies close to 100 MHz, well above the typical values reported for competing low-temperature thin-film technologies, such as organic TFTs. Higher frequencies can even be envisaged for similar L by employing reduced overlaps between gate and source/drain electrodes or even self-aligned structures. R_{ON} evolution with L shows that contact resistance is not affecting device performance even at L = 3 μm. Still, notorious SCEs (CLM and DIBL) are evident from the *I–V* characteristics when L$\leq$ 5 μm, resulting in negative V_{ON} and humps in transfer characteristics. Even if the physics behind these effects is still being studied in detail, the present study provides valuable information to circuit designers regarding device performance evolution in a large L range, showing the potential of oxide electronics for low temperature and large area flexible circuits operating in the MHz range.

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