Design Tradeoffs for Voltage Controlled Crystal Oscillators with Built-in Calibration Mechanisms

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***Abstract*—Timing is a critical issue in communication systems, especially for synchronous communications. These show a high dependence on the clock signal purity due to errors that can be introduced into the decision process. This paper addresses the design, on a 130nm CMOS process, of a *Radiation Tolerant Voltage Controlled Quartz Crystal Oscillator* (VCXO), including techniques to reduce the influence of radiation and noise on its performance. The VCXO is included on a PLL designed to work within *High Energy Physics* (HEP) experiments.**

***Index Terms*—Voltage Controlled Quartz Crystal Oscillator, Phase-Noise, Crystal, Radiation Tolerant, High Energy Physics, Large Hadron Collider**

I. Introduction

The continuous growth of digital communications demands for higher speed serial communication circuits. Phase-locked loops (PLL) are critical elements of these circuits, as these are responsible for the generation of clock signals. These are required to show low phase noise, low jitter, and low frequency drift to transmit low noise data streams, from which clock is recovered to sample data in the receiver. The output data jitter, generated mainly by the voltage controlled oscillator (VCO) and partially filtered by the PLL, is one of the most important transmitters' figure of merit. Jitter degrades also during circuits' mission due to ageing, power supply variations and environmental effects.

High energy physics (HEP) experiments carried-out in the Large Hadron Collider (LHC) at CERN require capturing, transmitting, and processing a large number of sensors' signals. Phase-Locked Loops are used in these electronic systems for clock reference generation, clock data recovery, and to suppress jitter on timing distribution systems. Due to the high levels of radiation involved in these experiments, front-end electronic circuits must be hardened to minimize the likeliness of occurrence of functional errors or even irreversible defects.

The effects of irradiation on electronic circuits are divided mainly in short-term or Single-Event Effects (SEE) and long-term or Total Ionization Dose (TID) effects. The latter are due to cumulative effects and are responsible for changes in the electrical behavior of MOS circuits due to the trapping of positive charges in the oxide and semiconductor-insulator interfaces, which can render an increase of leakage current, a reduction of mobility, and a significant threshold voltage shift.

These unwanted effects to which circuits are exposed, is a motivation to measure, quantify and act against the multiparameter deviations caused by these external factors. This can be achieved with the use of Built-in Self Test circuits (BIST) [1] [2]. BIST circuits are integrated in nowadays electronics design. Among all the calibration/auto-calibration features, BIST circuits can, as well, be used to correct the operation of a circuit due to variations induced by electrical, temperature, radiation and other undesired phenomena.

When a signal is received the VCXO switches to full power and full performance mode, with lowered phase noise. Comparing to a typical standby mode where the VCXO would be switched-off, maintaining it in operating mode, having the MOSFET in Weak Inversion, allows a faster settling time, i.e. a faster switching from standby to normal operation.

The work presented herein addresses the design of a low-jitter, low-power and radiation hard Voltage Controlled Crystal Oscillator (VCXO) to be used in high performance PLLs for HEP electronics systems. This requires considering the intrinsic and extrinsic noise and radiation robustness properties of potential candidate oscillator circuits. For their characteristics with respect to low phase noise and power, quartz crystal based oscillators are considered. As the crystal element cannot be integrated, the evaluation of the VCXO has to consider these two elements separately: the crystal and the IC design.

This paper is organized in seven sections: the second section gives a short introduction on phase-noise; the MOSFET in weak inversion is discussed in section three; the full circuit is described in section four; the calibration mechanisms are described in section five; sixth section presents some design tips; section seven draws the main conclusions.

II. Phase-Noise in VCOs

An oscillator's phase-noise is a random frequency modulation close to the carrier (close-in frequencies) by different and eventually inter-related noise sources, namely, thermal noise and flicker noise. The use of crystal resonators (with very high Q), which allow squeezing the bandwidth around the carrier frequency, and the reduction of noise sources amplitudes, are the two main procedures to reduce oscillation phase jitter.

A first equation to model phase-noise was presented by D. B. Leeson [3].

$$L(\Delta\omega) = 10 \cdot log \cdot \left[\frac{2FkT}{P_{sig}} \left(1 + \left(\frac{\omega_0}{2Q\Delta\omega} \right)^2 \right) \cdot \cdot \left(1 + \frac{\Delta\omega_1 / f^3}{|\Delta\omega|} \right) \right] \quad (1)$$

where $L(\Delta\omega)$ is the value for the phase noise in dBc/Hz, F is a fitting factor, P_{sig} is the average power of the signal, k is the Boltzmann's constant, T the absolute temperature, ω_0 is the central frequency and $\Delta\omega$ is the offset relative to the carrier.

Despite relying on the fitting parameter (*F*) and on the empirical extension for the $1/f^3$ region, equation (1) gives insight on the relationships between the parameters that contribute to phase-noise in oscillators. From (1) it can be seen that, increasing the power of the signal phase noise decreases, which generally is accomplished at the cost of higher power dissipation. Second, the quality factor Q has a major impact on phase noise: increasing the resonator Q value results in improved phase noise. Third, reducing $1/f$ noise contribution, by proper choice of transistor type parameters, can limit the close-in phase noise.

978-1-4799-3525-3/13/$31.00 ©2013 IEEE

Equation (1) can be an useful starting point for the designer, in order to give a guideline of how critical is the value of one parameter over the other. From the referred equation, there is a visible trade-off between power and phase-noise, which can demand the need for a mechanism to control the current on the oscillator, and hence the power. Implementing a current steering circuit, allows the proper operation after the fabrication of the circuit (VCXO).

III. MOSFET IN WEAK INVERSION

As seen in section II, noise minimization demands, in a first approach, high power consumption and an high Q.

The most intriguing form of noise is the flicker $(1/f)$ noise. Flicker noise nature is yet not completely understood and in MOSFETs it is directly related to surface-sensitivity phenomena [4].

A bias switching to make the MOSFET work from accumulation to strong inversion to reduce $1/f$ noise in MOSFETs was proposed in [5]. It is known that the signal-to-noise ratio is worse in weak inversion than in strong inversion. However, a compromise can be found for the power consumption and phase noise tolerated by each circuit.

The MOSFET can operate, mainly, in two inversion regions: strong and weak. The strong inversion has the advantage of offering small aspect ratios and a large bandwidth, but a poor transconductance efficiency ($\frac{g_m}{I_D}$). On the other hand, weak inversion provides lower bandwidth, large aspect ratios and a higher transconductance efficiency. It is known that the signal-to-noise ratio is worse in weak inversion than in strong inversion. As in weak inversion a MOSFET behaves accordingly to an exponential law, just like the BJT, a similar equation can be written for the MOSFET (2), but affected by a slope factor n.

$$I_D = I_{D0} \cdot \frac{W}{L} \cdot e^{\frac{V_{GS}}{n \cdot U_T}} \tag{2}$$

where I_D is the drain current, I_{D0} is a process dependent constant and U_T the thermal voltage.

The most intuitive way for the designer to work with weak inversion is using the *Inversion Coefficient* (3) as shown in [6].

$$IC = \frac{I_D}{2n_o\mu_o C'_{ox} U_t^2 \left(\frac{W}{L}\right)} = \frac{I_D}{I_o \left(\frac{W}{L}\right)} \tag{3}$$

The definition of IC allows the designer to immediately obtain the values for I_D,*W* and *L*, which are the starting point for any design. So the designer, usually starts by choosing the IC value and the L. If $IC < 0.1$, the transistor operates in weak inversion; for $IC > 10$ it is, then, operating in the strong inversion. The gap between the two: $0.1 \leq IC \leq 10$ is called moderate inversion, having its center for $IC = 1$.

To guarantee operation in weak inversion and saturation, the MOSFET must have $V_{EFF} < -72\ mV$, for a given technology [6]. This condition only assures that the transistor is operating on the edge of weak inversion, but in order to be saturated, $V_{DS} \geq 4U_T \approx 104\ mV$.

The operation in weak inversion gives the best $\frac{gm}{I_D}$ performance, but on the other hand the worst *signal-to-noise ratio*. Despite being governed by an exponential law, just as the bipolar transistors, the nature of flicker noise in each device is different, resulting on a worse phase-noise in weak inversion.

IV. VOLTAGE CONTROLLED OSCILLATOR TOPOLOGY

A. Topology

This work requires the design of VCXO capable of low-phase noise and low-power capabilities. The circuit's topology is crucial to meet these requirements, as they inject noise in different instants and the power consumption varies from on to the other.

The well known model Three Point Oscillator (TPO), proposed by Vittoz [7] (Fig. 2) can be converted into three different topologies just by changing the grounding node: Colpitts, Pierce, or Santos.

The most common topology in crystal oscillators is the Pierce oscillator. In this topology the tuning capacitors are grounded, allowing these capacitances to absorb the parasitic capacitances (such as the transistor's drain- and gate-source capacitances). In the Colpitts and Santos oscillators the crystal is grounded, which contributes to added parasitic capacitances in parallel to the crystal [8]. Finally, Pierce topology allows the use of crystals up to 200 MHz [9].

The TPO can be divided into the motional branch of the crystal and the circuit with all parasitics included. Fig. 3 shows the Pierce configuration (chosen for this work) with the addition of variable capacitors to allow for frequency tuning. The capacitive network together with the active device are responsible for generating the negative resistance that assures the start-up condition and sustains oscillations. To ensure sufficient tunning range, the variable capacitance is implemented by combining a load digitally programmable capacitance (C_{bank}) for coarse frequency tuning and a varactor (C_{var}) for fine tuning by means of a continuous voltage (Fig. 1).

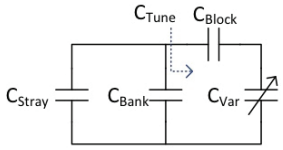

Fig. 1. Tuning Network

This combination allows for coarse and fine tuning, in order to cover all the frequencies' range within the specifications. As the equivalent load is finite ($\approx$ 30 pF maximum), it is possible to achieve some controlled tuning of the frequency. Note that all stray and tunning capacitances are accommodated into this value. A blocking capacitor C_{block} (Fig. 1) is used to isolate the varactor control voltage from biasing.

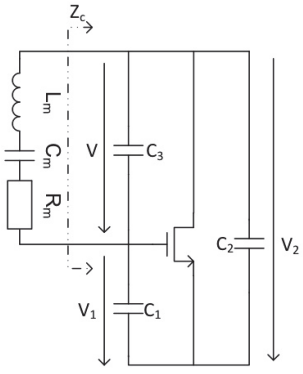

Fig. 2. TPO

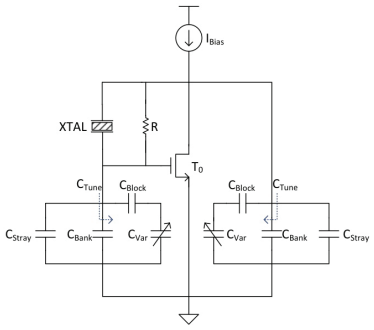

Fig. 3. VCXO

Digital Tuning

Digital (or coarse) tuning of the VCXO is accomplished using a binary weighted bank of capacitors (Fig. 4) with a resolution of seven bits. When all enable pins are set the maximum load capacitance of 20 pF is achieved, otherwise if all the bits are off the remaining capacitance is the parasitic capacitance ($\approx$ 30 fF) worth about $\frac{1}{10}$ LSB of the bank of capacitors resolution.

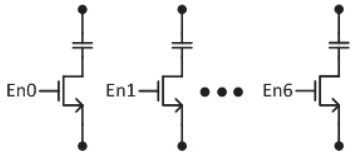

Fig. 4. Bank of Capacitors.

Analog Tuning

Analog/fine tuning is achieved using a varactor. As the varactor is in series with the blocking capacitance, the former limits the varactor's excursion.

From the technology used, with the controlling voltage varying from 0 to 1.5 V, the varactor's capacitance is given by $C_{var} = k \cdot C_{block}$, where k is a technology dependent parameter.

For a blocking capacitance value of 31 pF, the varactor actually varies between ≈ 3 pF and 14 pF. The tuning ranges obtained are plotted in Fig. 5.

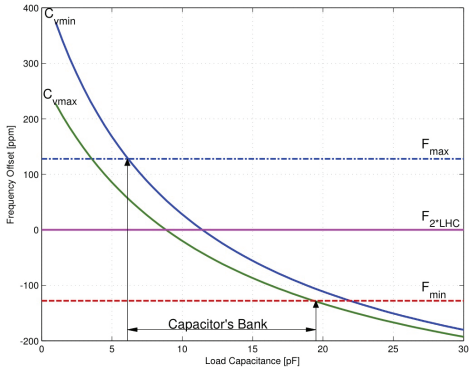

Fig. 5. Tuning Range

The points F_{max} and F_{min} correspond to $\approx \pm 130ppm$ limits of frequency offset. The intersection of F_{max} with the curve for maximum C_v ($max[C_v]$), gives the minimum value for the capacitor's bank ($min[C_{bank}]$). The same is applied to calculate $max[C_{bank}]$.

The calculation and plot of Fig. 5 has been done based on the simulation of behavioural equations using Matlab. As it is known, the quartz crystal imposes a very narrow bandwidth of operation to the VCXO, due to its high quality factor, thus the variation achieved by the varactor is in the order of *ppm* and it is not visible on a transient simulation. For this type of oscillators, the equations given in [7] added with the technology data, suffice to design accurately a crystal oscillator.

B. Start-up conditions for oscillation

The transistor's biasing level is, in first place, determined by the oscillation start-up conditions. Dividing the oscillator in two main parts (Fig. 2): the crystal motional circuit and the active electronic circuit, in order to start oscillations the active part must be capable to compensate for the losses in the motional circuit (represented by R_m), what is know as negative resistance. Calculating the impedance of the circuit, a bilinear function of g_m is found, where g_m varies from 0 to ∞. According to [7] there are two possible conditions for oscillation: points *A* and *B* (Fig.6).

A sustained oscillation can only be achieved in point *A* since *B* is not stable [7]. The g_m value at point A (g_{mcrit}) corresponds to the minimum transconductance that ensures stable oscillations and

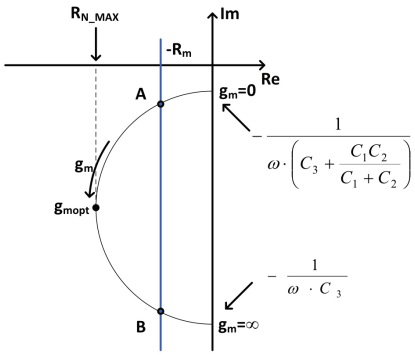

Fig. 6. Representation of impedances on the complex plane [7], [8].

is given by equation (4). The maximum g_m that can be set in the oscillator (g_{mopt}) corresponds to the magnitude of minimum value of negative resistance that can be developed by the circuit. If the losses to be compensated by the active device exceed the maximum negative resistance the system will not oscillate, even if the g_m is increased indefinitely. Consequently, the circuit's transconductance should be in the range $g_{mA} \leq g_m \leq g_{mopt}$, and the losses must lie on the complex plane semi-circle.

$$g_{mcrit} = \frac{\omega}{Q \cdot C} \cdot \frac{(C_1C_2 + C_2C_3 + C_3C_1)^2}{C_1C_2} \tag{4}$$

The negative resistance for the maximum load ($C1 = C2 = 30pF$) has been evaluated. The results in Fig. 7 show that the oscillator in Fig. 3 is capable of compensating the losses of the resonant circuit (R_m), in this case, $R_m = 35\Omega$ being the worst case value.

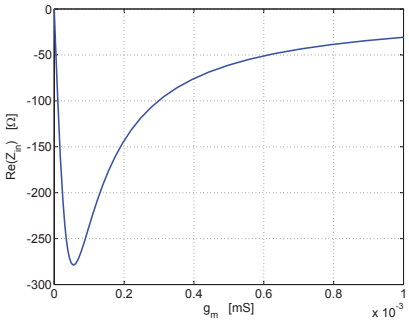

Fig. 7. Negative resistance as a function of g_m.

C. Biasing

A variation of the circuit load corresponds to a variation on the current flowing in the oscillator. A current switching scheme together with an offset current (Fig. 8), ensures the operation of the circuit for diverse load values or PVT variations (this circuit is represented by I_{bias} in (Fig. 3)). The minimum current sourced by the offset current source (always on) is 500 μA. The binary switching of the current allows increasing this value up to 3 mA, giving the VCXO the ability to operate with a large variation of the applied load. Thus, the maximum power consumed by the VCXO 4.5 mW.

The circuit, includes a g_m-*constant* biasing circuit [10], responsible for generating the reference current for the circuit in Fig. 8.

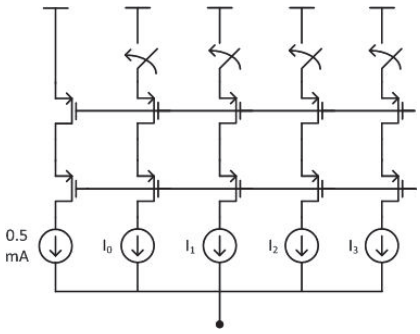

Fig. 8. Current steering.

D. Comparison between inversion regions

To finalize this section, both strong and weak inversion are compared. As expected the phase-noise/jitter in weak inversion is worse than in strong inversion, due to its lower signal-to-noise ratio.

However, the results obtained can give some guidance, according to the application being developed. A decay of the Cycle-to-Cycle Jitter with the increasing power can be observed in both strong and weak inversions. From Fig. 9 and Fig. 10 it can be seen that there is a factor of two separating both inversion regions. The corresponding power consumptions, for maximum load, would be respectively $4.5\ mW$ and $2.2\ mW$.

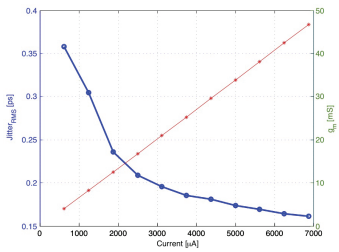

Fig. 9. Strong inversion.

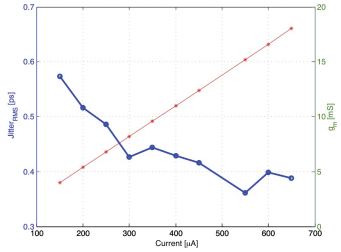

Fig. 10. Weak inversion.

On one hand, in the case of this specific oscillator it is clear that strong inversion would be more adequate to meet the principal goal - low noise. On the other hand, weak inversion would allow a fast recovery from a *stand-by* mode. In this particular circuit, the use of a cascode PMOS current steering, that by itself stabilizes the common-mode point generating less flicker noise, can be complemented placing these tail mosfets operating on the edge of weak inversion [11].

Other applications, can obtain very good results operating entirely on the weak inversion region, when low power consumption is the primary concern.

E. Quartz Crystal

Since a crystal oscillator comprises a quartz crystal and an electronic circuit, it is important to assess to what extent the quartz crystal itself is affected by radiation. To evaluate the crystal's sensitivity to radiation six samples out of a group of seven were irradiated. The quartz crystals where irradiated with 60 MeV neutrons with fluencies up to 3E15 n/cm2.

Table I shows the results of the crystal frequency deviation. The first entry in the table corresponds to a non-irradiated device that was used as a reference to control the post-radiation measurements. The data shows that the frequency shift is positive and that in all cases it is bellow 8 ppm. The devices tested were manufactured for a frequency tolerance of ± 18 ppm and for a frequency drift over the operating temperature range that should not exceed ± 10 ppm. From the measurement data, it can be concluded that the crystal is radiation hard since the frequency drift due to radiation is a fraction of the manufacturing plus temperature drift tolerances.

TABLE I
RESULTS OF THE RADIATION TESTS ON THE CRYSTAL

XTAL	Dose [n/cm2]	Δf [Hz]	Δf [ppm]
R	0	-10	0
1	6E+14	68	2
2	3E+15	308	8
3	3E+15	330	8
4	6E+14	229	6
5	9E+14	141	4
6	9E+14	96	2
$< \Delta f >$		195	5
σ		111	3
MAX		330	8

F. Layout

In Fig. 11, the layout of the full VCXO is detailed. It is visible that the layout is symmetric, which improves the low-noise performance [12].

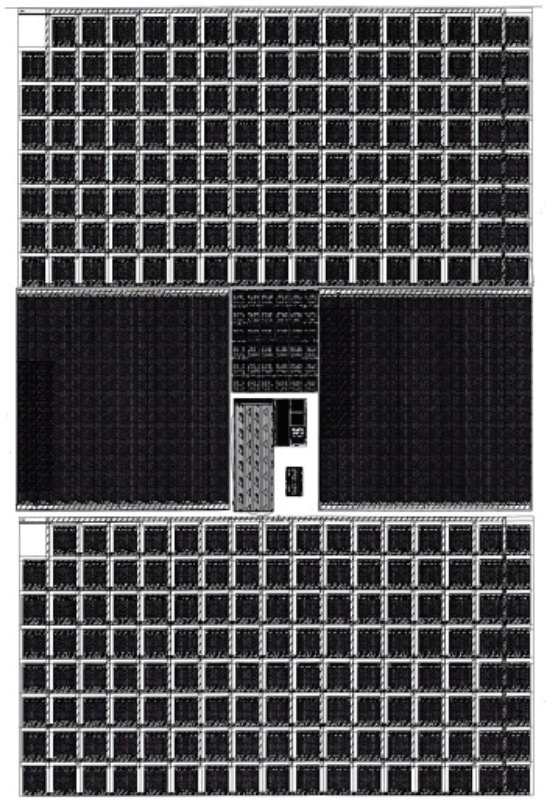

Fig. 11. Layout of the VCXO

The layout includes digital tuning blocks (top and bottom of the figure), varactors visible on the center (left and right) and in the center the biasing circuitry and the VCXO. Common techniques were used, such as: the use of dummy cells; common centroid layout and the use of guard-rings for circuit protection against the effects of radiation [13].

The use of guard-rings and Enclosed Layout Transistors (ELT), reduce the effects of TID on circuits. However, in this work, ELTs are not used, once with the decrease of the technology node the number of positive charges trapped in the interface decay quadratically with the thickness of the oxide. The major concern are now the SEE which can only be avoided making use of techniques such as triple voting.

V. Calibrating Mechanisms

The two techniques described previously in section IV, analog tuning and digital tuning, are used on the circuit with the purpose of calibration, as it can be seen on Fig. 12. An external set of building blocks has been used along with the referred VCXO, in order to interface with the tuning mechanisms. The building blocks used to control, both fine and coarse tuning, are mostly digital and actuate on the VCXO through an external circuit. This way, we can say that the VCXO, Amplitude Oscillation Control, Frequency Detector and the Test Circuit, form a loop in order to correct deviations during operation.

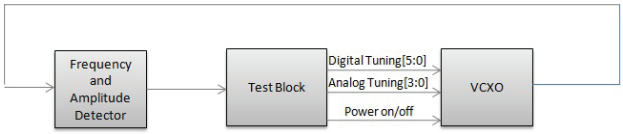

Fig. 12. Calibration Mechanism

In first place, the calibration circuit receives as an input the amplitude and frequency of the oscillations. From here, the it will correct the VCXO behaviour using analog and digital tuning.
Analog tuning will provide control over the current flowing through the *VCXO*, enabling to choose the operating region of the MOSFET and to cope with the load imposed to the circuit. The current variation is set by a digital word that controls the fine tuning structure presented in Figure 5.
The variation of the VCXO bias current, affects a diversity of parameters:*gm* of the transistor (hence the gain); operating inversion region; maximum admissible load ; and trade-off between power and phase-noise. All of this can be accomplished, using one single calibration block.
Depending on the operating mode, the VCXO can run either at very low power levels or at a very low phase-noise. For some applications a balance between the two is needed, which is as well possible with this calibration mechanism.

Digital tuning is a coarse tuning used to set the operating frequency of the *VCXO*. A bank of binary weighted capacitors is used, which allows to correct frequency deviations of each circuit, due to PVT variations during the fabrication process. The use of a very high *Q* resonator (crystal resonator), which allows minimum frequency deviations, will demand a much higher load when compared to standard, low Q, tank circuit. This increase of the load of the circuit, will require more power so the circuit can operate, which is controlled by the fine tuning circuit, that will source more current to the circuit.
As a conclusion, the fine tuning mechanism focus, mainly, in maintaining oscillations delivering the correct amount of gain that generates the needed gain. The coarse mechanism acts on the oscillator's frequency. However as the load varies, the fine tuning circuit, must adapt the gain of the mosfet, so the oscillator works in every condition.

Regarding the region of operation of the circuit, as it can be seen from Fig. 10 and Fig.9, in weak inversion the jitter observed is two times worse than in strong inversion, however the consumed power is ten times less. For our particular circuit a good compromise was obtained on the beginning of strong inversion ($IC = 10$).

VI. Tips for the Designer

In the previous sections all the fundamental concepts necessary for design a balanced design were explained.

The radiation-induced effects on circuits can significantly increase flicker or $1/f$ noise in CMOS devices, which is detrimental to the phase noise of front-end circuits [14].

The designer can effectively reduce phase noise by means of increasing the power delivered to the circuit and the quality factor (Q). To overcome increasing power, a careful layout should be designed taking into account perfect symmetry and proper decoupling. Using this approach the designer can control $1/f$ noise, thus its modulation to close-in frequencies [12].

Regarding low power design, operation in weak inversion for very power sensitive circuits can be used. But here lays a trade-off between power consumption, and the not so good noise performance in weak inversion. The decision on which region the circuit should operate in must be taken case by case.

In the circuit being proposed, operation in the onset of strong inversion has been chosen. The circuit has been simulated operating also in weak inversion, but the obtained phase noise results are two times worse. Fig. 9) and Fig. 10 show the variation of phase-noise with power consumption.

Besides the design techniques explained previously, a current steering mechanism has been included in the VCXO. This mechanism allows to both assure start-up conditions, and diminish the start-up time of the circuit. As seen in Fig. 8, the switches can be on and off according to the circuit needs. Besides that, a constant current of $500\ \mu A$ flows through the VCXO, defining the worst case scenario, that is the maximum value for the phase-noise using a given load. Regarding radiation tolerance, the current control allows a faster recover to a steady state operation when a sensitive node of the oscillator is affected by a high energy particle hit.

VII. Conclusion

A low-noise radiation tolerant VCXO with a tuning range of $\pm 8kHz$ around nominal frequency, to be integrated into a PLL and used in HEP experiments, has been designed. The VCXO topology is based on a Pierce oscillator biased in strong inversion. The circuit has control mechanisms, which allow varying the current on the VCXO, in order to guarantee the start-up condition regardless load or PVT variations.

The layout of the circuit was designed taking into account symmetry as referred in [12] and is presented in Fig. 11. The operation of the VCXO was simulated in both weak and strong inversion. The choice of the operating region has to take into account several variables: exposure to radiation, power consumption, power delivered to the crystal, and phase-noise. These tradeoffs must be decided by the designer on a case by case basis.

Acknowledgment

The authors are thankful to CERN for the facilities and support given to this project, in particular to Dr. Paulo Moreira for his contribution to this project and to Mr. Karl Gill for setting up the irradiation campaign.

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