A Complementary LC-tank Based IR-UWB Pulse Generator for BPSK Modulation

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Abstract

This paper presents a low-power binary phase shift keying (BPSK) pulse generator for ultra-wide-band transmitters. The circuit has been designed based on LC-tank resonators using 0.13 um CMOS technology. Simulation shows -10dB bandwidth of around 3 GHz and power consumption of 2 mW at 100 MHz PRF. Peak-peak amplitude voltage for both symbols '1' and '0' are approximately as large as 1.2V supply voltage and can radiate enough energy to satisfy the FCC mask only by one pulse. Thus, the energy consumption is 20 pJ/pulse/bit. Pulse duration is 1.5 ns and the transmitter can reach data rates of 660 Mbps

1. Introduction

UWB frequency range (3.1-10.6 GHz) was released and defined by the Federal Communications Commission (FCC) in 2002 as an unlicensed frequency band at a limited Effective Isotropic Radiated Power (EIRP) of -41.3 dBm/MHz in order not to interfere with narrow-band systems like GPS, Personal Cell Systems (PCS), Bluetooth, etc. [1], [2], [3]. After a decade, this frequency range has lost its interests for mobile communication mostly due to limited transmission power/range. However, still it can be used in other specific applications, e.g. wireless sensor networks (WSN), biomedical implants and internet-of-things (IoT).

Impulse-Radio UWB (IR-UWB) is one of the most suitable communication techniques for UWB low-power applications, which uses a short-duration pulse with large bandwidth and known as a carrier-less technique. Not using up and down conversion, IR-UWB transmitters have low complexity in architecture, leading to less power consumption, less die area and lower production cost. These properties make UWB transceivers eminently suitable for sensor nodes in IoT and WSN [2], [4].

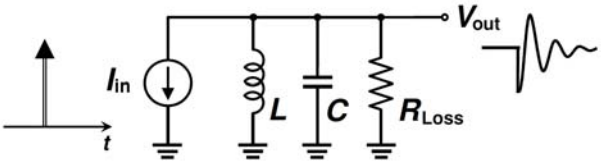

Figure 1. Decaying oscillatory behavior of a lossy LC tank triggered by a current impulse [6]

Different modulation techniques can be used in IR-UWB transmitters, such as binary phase-shift keying (BPSK), pulse-position modulation (PPM), and on-off keying (OOK). BPSK (a.k.a. biphasic) is suitable for smooth spectrum usage and it has a better bit error rate (BER), but usually channel estimation is required and the architecture of the system becomes large and complex due to coherence requirement. Contrarily, OOK and PPM are based on the presence and absence of the pulse and no channel estimation is required. Compared to BPSK, OOK and PPM have less BER [4], [5].

A variety of techniques have been used to design IR-UWB BPSK pulse generators, from all-digital techniques [7] to LC-VCO based [8], [9] and mixer based circuits [10], [11]. The work introduced in [12] has used two ring oscillators triggered by positive and negative signals. Combination of delayed triangular glitches [13] and Step Recovery Diode (SRD) based circuits [14] also have been presented in literature. Another approach is to apply a glitch (spike) to a filter network [15], [16], [17] such that it forms a UWB impulse at the output; however, using complex filters and drivers has led to higher power consumption. In [16], although 1.93 pJ emitted energy per pulse is reported, the circuit dissipates 393 pJ to generate a single pulse. The very last technique also can be seen as usage of decaying oscillatory behavior of an RLC network, which is the fundamental idea used by the proposed IR-UWB pulse generator in this paper.

The rest of this paper is organized as follows. In section II, the proposed pulse generator has been

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introduced. In section III, simulation results will be discussed, followed by a conclusion in section IV.

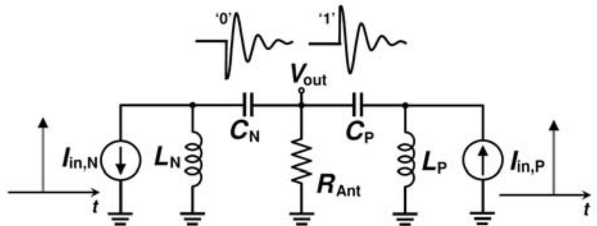

Figure 2. A complementary circuit can invert the direction of impulse so that the polarity of the output voltage will be reversed.

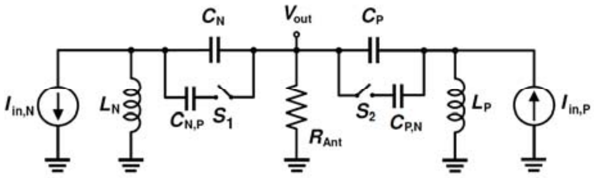

Figure 3. A complementary tank can be used as a filter for 1.6 GHz frequency if the value of the capacitor changes.

2. Proposed Pulse Generator

As illustrated in Fig. 1, a lossy LC tank triggered by a current impulse shows a decaying oscillatory response. In fact, the resistance of the capacitor and the inductor converts into heat some of the energy that reciprocates between them. This concept can be used for designing a very low power pulse generator, mainly because there are not many components in such a circuit. The UWB pulse generator is supposed to drive a 50 ohm antenna, therefore in the RLC network the R_{Loss} can be replaced by R_{Ant} = 50 ohm. In power spectral density (PSD), the central frequency is defined as ω_o = 1/sqrt(LC) and how fast or slow the signal decays will determine the bandwidth. The faster it decays, the wider bandwidth will be obtained.

By adding a complementary circuit (Fig. 2), the direction of the current through R_{Ant} can be reversed so that it creates a pulse with opposite phase that serves BPSK modulation. The capacitor comes in series in the RLC network in order to better filter out the low frequency components of the input impulse. In the positive half circuit including $I_{in,P}$, L_P and C_P, the complementary negative LC tank, including L_N and C_N, would easily kill the signal because it oscillates at the same frequency. Yet, they can be seen as a series LC filter to suppress the frequencies around 1.6 GHz where FCC rules are more strict because of satellite and GPS band [1]. Thus, the capacitance C_N should increase by using a larger capacitor $C_{N,P}$ coming in

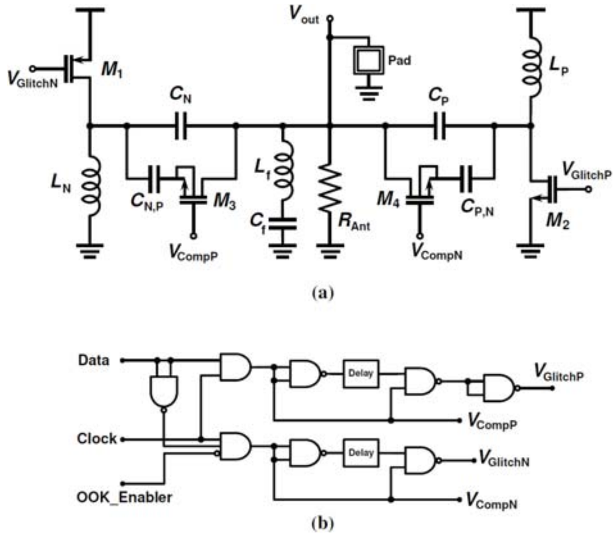

Figure 4. Proposed IR-UWB modulator. (a) Complementary pulse generator, (b) Control signals and glitch generator.

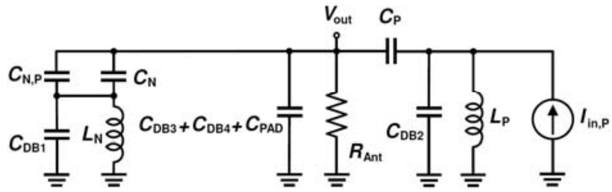

Figure 5. Half circuit model of the positive pulse generator

parallel with it, shown in Fig. 3. The combination of $C_{N,P}$ + C_N and L_N forms a series LC network oscillating at ω_o = 1/sqrt[L_N * ($C_{N,P}$ + C_N)]. If $C_{N,P}$ is chosen properly this network can diminish the power of signal around 1.6 GHz frequency band. Contrarily, a complementary impulse can be applied to the negative half circuit. Similar to the positive half circuit, same phenomena exist for negative half circuit that creates an oscillation using L_N and C_P, and the $C_{P,N}$ and C_P are used for filtering lower frequency components. Considering that $C_{N,P}$ should not be present in the negative half circuit, a switch ,S_1, is used to disconnect it, while S_2 makes C_P and $C_{P,N}$ in parallel.

Knowing the above-mentioned concepts, the pulse generator can be implemented using CMOS technology. Demonstrated in Fig. 4(a), impulse sources are realized using MOSFETs triggered by glitches. Also M_3 and M_4 are utilized instead of S_1 and S_2, respectively. Figure 4(b) shows the positive and negative glitch generator circuits. The delay modules can be tuned in order to control the width of the glitches and therefore to adjust the power of pulses. Moreover, by setting the "OOK_Enabler" input to '1', the modulation will be converted to OOK because $V_{GlitchN}$ and V_{CompN} will be deactivated and the glitches are applied only to positive half circuit.

TABLE I
Performance summary of the proposed pulse generator and comparison

Specification	Praveen [15]	Na [7]	Muhr [16]	Xia [17]	Qin [18]	This Work
Supply Voltage	1.8 V	1.2 V	1.2 V	1.2 V	1.2 V	1.2 V
Energy consumption (pJ/Pulse)	86	30	393	44	33	20
Data Rate	250 MHz	200 MHz	10 MHz	100 MHz	1.3 Gbps	660 Mbps
-10dB Bandwidth (GHz)	3.5–6.5	0.5	1.8	3-5	3.1-10.6	3.3-6.2
Output Amplitude	0.5 V	0.4 V	1.72 V	0.24 V	86 mV	1 V
Peak PSD Power (dBm/MHz)	-42	-	-	-40	-	-40.4
Process (nm)	180	65	130	130	130	130

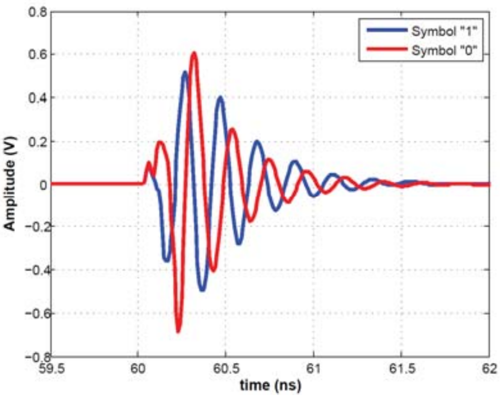

Figure 6. UWB pulse signals in time domain

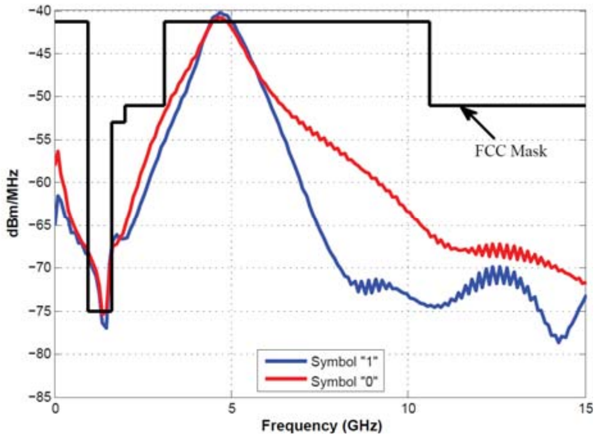

Figure 7. Output power spectral density (PSD) for both positive and negative signals

Positive half circuit model of the pulse generator is shown in Fig. 5. Since the capacitance value of C_N and C_P are too small and comparable to drain-bulk parasitics added by $M_{1\text{-}4}$, they degrade the frequency response of the circuit. Besides, adding a pad of the size 100 um × 100 um to the output node exacerbates it. Therefore, in order to compensate such undesired effects a series LC filter, including L_f and C_f, with resonance frequency around GPS band has been utilized.

3. Simulation Results

The proposed transmitter is implemented by 0.13 um CMOS process with 1.2 V supply voltage. BPSK modulation needs output pulses with 180° phase shift, shown in Fig. 6. If all input data is '1', the pulse amplitude is 1V and the overall power consumption of the pulse generator is only 1.9 mW, including 160 uW of the glitch generator circuit at 100 MHz pulse repetition frequency (PRF). On the other hand, if all input data is '0', at the same clock rate the pulse amplitude is 1.28 V and the power dissipation is 2 mW, resulting in 20 pJ/pulse energy consumption. The large amplitude of the output signals provides mask satisfaction by means of a single UWB pulse. Thus, the 20 pJ/pulse energy can be interpreted as the amount of power consumption per bit (20 pJ/pulse/bit). Illustrated in Fig. 7, both impulses have central frequency of 4.8 GHz. Using periodogram, PSD of the output signal has been calculated for 10 cycles of it where the window size has been chosen such that it roughly contains one period of UWB pulses (10.24 ns). The power of pulses can be controlled by the delay module in glitch generator circuit. The wider the glitches are, the larger the value of current spikes charging L_N or L_P inductors. Figures 9(a) and 9(b) shows the glitches applied to M_1 and M_2, respectively. For a glitch as wide as 45ps the peak power of pulses are around -40.4 dBm/MHz. The UWB pulse which corresponds to symbol '1' has -10dB bandwidth of 3.5-6 GHz, while the one for symbol '0' shows slightly larger bandwidth 3.3-6.2 GHz. Duration of each pulse is 1.5 ns which means the maximum PRF could be around 660 MHz. The performance summary of the proposed pulse generator along with a comparison with other published papers is listed in TABLE I.

9. Conclusion

A pulse generator with very high output amplitude (roughly as large as supply voltage) for BPSK modulation was presented. It achieves power consumption of 20 pJ per pulse while PSD estimation shows each pulse can satisfy the FCC mask and can be considered as one bit. Due to the loss of bond-wires and compensating the effects of process corners, the glitch generator circuit has been designed such that the PSD peak power (-40.4 dBm/MHz) can be tuned and controlled. Thanks to the PSD similarity of both "0" and "1" symbols, designing the low-noise amplifier at the receiver will not be complex and it needs to be designed for 3 GHz bandwidth with central frequency of 4.8 GHz. The proposed pulse generator also allows the communication using OOK modulation if required.

9. Acknowledgment

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