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InGaZnO TFT behavioral model for IC design

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Abstract This paper presents a behavioral model for amorphous indium–gallium–zinc oxide thin-film transistor using artificial neural network (ANN) based equivalent circuit (EC) approach to predict static and dynamic behavior of the device. In addition, TFT parasitic capacitances (C_{GS} and C_{GD}) characterization through measurements is also reported. In the proposed model, an EC is derived from the device structure, in terms of electrical lumped elements. Each electrical element in the EC is modeled with an ANN. Then these ANNs are connected together as per the EC and implemented in Verilog-A. The proposed model performance is validated by comparing the circuit simulation results with the measured response of a simple common-source amplifier, which has shown 12.2 dB gain, 50 μW power consumption and 85 kHz 3-dB frequency with a power supply of 6 V. The same circuit is tested as an inverter and its response is also presented up to 50 kHz, from both simulations and measurements. These results show that the model is capable of capturing both small and large signal behavior of the device to good accuracy, even including the harmonic distortion of the signal (that emphasizes the nonlinear behavior of the parasitic capacitance), making the model suitable for IC design.

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1 Introduction

In recent years, analog/mixed signal circuit design using a-IGZO TFT technology [3, 13, 15] is gaining significant interest because of its exceptional characteristics, such as relative high mobility, low-temperature and low-cost fabrication [4, 10, 11]. This demands accurate device models that can predict both static and dynamic behavior of the device during circuit simulations. However, most of the reported circuits are confined to employ either a-Si:H [15] or a-IGZO static models [3, 13] (only with overlap capacitance).

In general, the work reported on a-IGZO TFTs modeling is either from device physics [6, 14] or from electrical measurements [3], but most of these models are also confined to static behavior characterization. However, it is essential to have an accurate device model that can predict both static and dynamic behavior. Nevertheless, a device model describing both I–V and C–V characteristics is presented in [1]. Here, C–V is limited to only total gate capacitance (C_G) and no details were provided on the individual TFT capacitance components between different electrodes, namely, gate to source (C_{GS}) and gate to drain (C_{GD}), which are essential in circuit design. Another good contribution was given in [12] towards a full description of both components by adapting MOSFET SPICE Level 3 model to the particular case of the a-IGZO TFT. Nevertheless, this model is limited in nature, as it is unable to precisely predict the unique properties of the amorphous oxide semiconductors (AOS) present in the TFT, since it is mainly meant for the crystalline silicon.

The IGZO TFT technology is still in an emerging phase, experiments are being conducted to optimize the device performance by various means [5, 8]. In order to facilitate immediate circuit design, accurate device models with small development time are required. Though physical models are recommended for circuit design and statistical analysis, their development time is significantly high. Especially, when the technology is still emerging, it is quite challenging to develop physical models since whenever an effort is made for the device optimization, e.g. changing materials or processing conditions, the corresponding physical phenomena that influence the charge carrier flow should be characterized and modeled. Therefore, this paper proposes an accurate behavioral model using ANN based EC approach that avoids deep theoretical analysis about device conduction mechanisms, and through which a workable model is devised in the order of minutes. In the proposed model EC is derived from the device structure (Fig. 1(a)). Consequently, this model cannot be treated as pure empirical, despite it is being developed solely from the device measured characteristics.

The EC of the device (TFT) consists of parasitic elements between different electrodes and a dependent current source that represents the current between drain and source, as shown in Fig. 1(b). Since the bulk (glass) is an insulator, there are no significant parasitics associated with it and can be neglected as their contribution in determining the dynamic behavior of the transistor is trivial. On the other hand, it is crucial to include device capacitance components between different electrodes (C_{GD} and C_{GS}) as Fig. 1(b) shows. Since the proposed model is developed from device measurements, it is essential to extract measured data for both C_{GD} and C_{GS}. Most of the articles reported the total gate capacitance ($C_{G\text{-}DS}$) of a-IGZO TFTs at different frequencies [7] and different bias voltages [1]. However, to the best of authors knowledge individual intrinsic capacitance ($C_{GSi} = C_{GS} - C_{OV\text{-}GS}$ and $C_{GDi} = C_{GD} - C_{OV\text{-}GD}$) characterization and modeling in the complete operating region of the transistor has not yet been addressed in literature for this TFT technology, which is essential for circuit design, in order to predict its frequency dependent behavior. This issue is also addressed in the present paper by characterizing the intrinsic capacitance of the device from measurements.

Once all the measurements are available for the drain current (I_D), C_{GD} and C_{GS}, a separate ANN is developed for each element to achieve good accuracy. Then, the device model is obtained by joining these three ANNs as per the EC. This model is then implemented in Verilog-A for circuit simulations. Later, the model performance is validated through a simple common source (CS) configuration, operating as an amplifier and an inverter (which is a fundamental block in the IC design) by comparing circuit simulation results with the measured response.

Section 2 gives details on the device characterization including capacitance measurements. Section 3 presents the device modeling. Section 4 shows experimental results and discussion and finally main conclusions are drawn in Sect. 5.

2 Device characterization

In this work, device static and dynamic characterization is done through measurements as a first step. Devices used for this end are similar to the ones reported in [3], i.e., staggered bottom gate IGZO TFTs with Ta_2O_5—based multilayer/multicomponent dielectric, annealed at 200°C. I–V and C–V characteristics are measured with Keithley 4200-SCS parameter analyzer at room temperature. Figure 2 presents the transfer characteristics of the TFT with W = 640 μm and L = 20 μm. These devices are showing a turn-on voltage (V_{on}) of −0.7 V, a threshold voltage (V_{TH}) of ∼1.35 V, on-off ratio greater than 10^7 and mobility

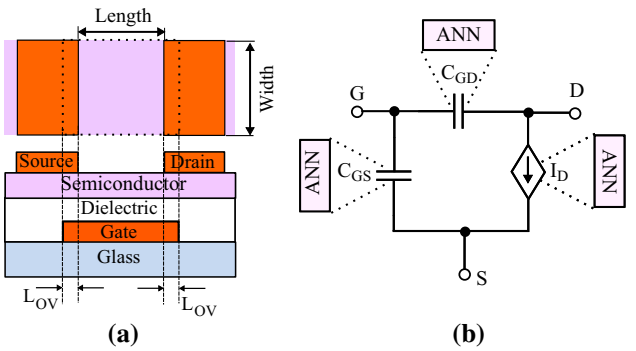

Fig. 1 a-IGZO TFT **a** Schematic. **b** Equivalent circuit of the device, in which individual elements need to be modeled with ANNs

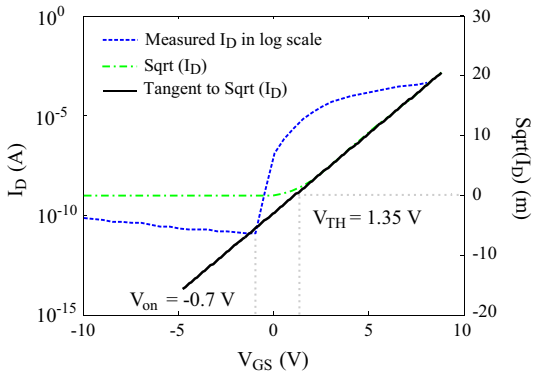

Fig. 2 IGZO TFT transfer characteristics showing $V_{on} = -0.7$ V and $V_{TH} \sim 1.35$ V

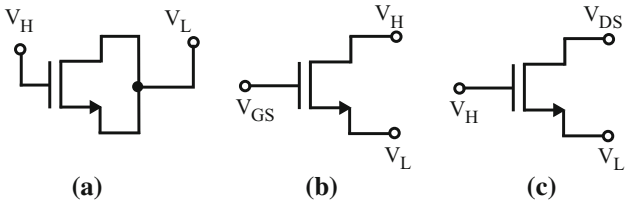

Fig. 3 Test setup to measure capacitance between different electrodes of a device: **a** $C_{G\text{-}DS}$. **b** C_{GD}. **c** $C_{GS} + C_{GD}$

around 20 cm^2/V s. All the devices in this work have a gate to drain/source overlap of 5 μm and a channel length of 20 μm.

2.1 Capacitance measurements

The total gate capacitance ($C_{G\text{-}DS}$) of the TFT is measured with the test setup shown in Fig. 3(a). In this measurement, the source and the drain of the TFT are electrically shorted, and connected to the ground terminal (V_L) while the gate is connected to the high terminal (V_H) of the Capacitance Voltage Measurement Unit (CVU). A dc voltage sweep of −6 to 6 V in steps of 0.5 V is applied to the gate, with an ac signal of 100 mV rms superimposed to the bias. The C–V measurements are repeated for different frequencies ranging from 30 to 500 kHz. The resulted C–V characteristics for a TFT wtih W = 640 μm is shown in Fig. 4. From these measurements it can be noticed that the total overlap capacitance ($C_{OV\text{-}GS} + C_{OV\text{-}GD}$) due to the overlap between gate to drain/source electrodes is ∼3.7 pF and the channel capacitance ($C_{CH} = C_G$—overlap capacitance) ∼3.3 pF. It can also be noticed that the measured capacitance is almost independent of the input signal frequency, at least within the applied signal frequency range. Therefore, for the other C–V measurements, an input ac signal with 30 kHz frequency is applied.

C_{GD} can be directly measured with the test setup shown in Fig. 3(b), where a dc bias is applied at the gate and signal is applied at the drain. Under this test setup, the gate acts as ground for signal, allowing for direct measurement of C_{GD}. On the other hand, Fig. 3(c) determines $C_{GS} + C_{GD}$, as drain acts as ground for signal. By subtracting C_{GD} from these values, C_{GS} can be determined. Intrinsic capacitances (C_{GSi} and C_{GD}) between different electrodes of the device are obtained by subtracting the overlap capacitance from C_{GS} and C_{GD}. Figure 5 shows the respective measurement results, revealing a close agreement with Meyers FET capacitive model [9] i.e., in the linear region $C_{GSi} = C_{GDi} \sim \frac{1}{2} C_{CH}$ and in the deep saturation, $C_{GSi} \sim \frac{2}{3} C_{CH}$ and C_{GDi} approaches to 0.

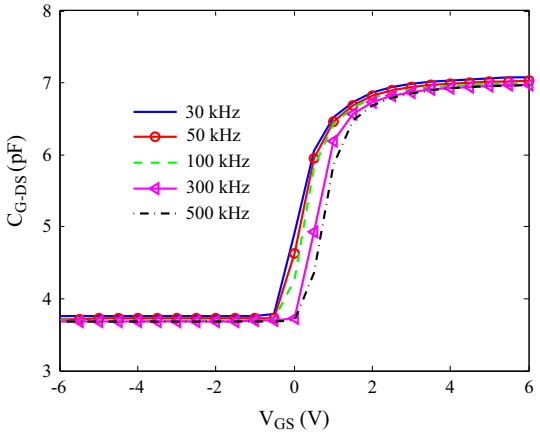

Fig. 4 Measured $C_{G\text{-}DS}$ at various frequencies, for a gate voltage sweep from −6 to 6 V in steps of 0.5 V

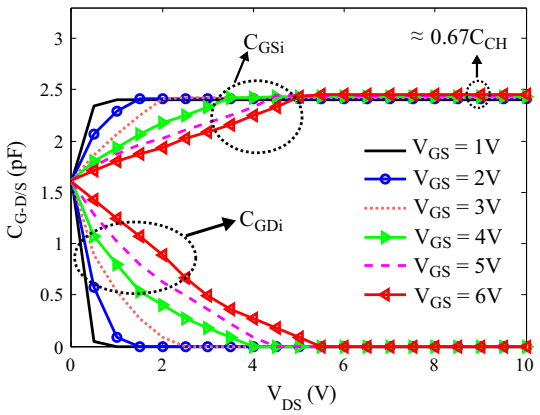

Fig. 5 Measured C_{GSi} and C_{GDi} for varying bias voltages

3 Device model

ANNs are good candidates for function estimation problems. ANN architecture corresponds to that of a parallel computing machine, formed from the interconnection of a set of artificial neurons. Each neuron in the network, commonly known as processing element, has a set of inputs, synaptic weights and bias. Training samples are applied at the input layer of the network so that it can learn the underlying physical process, subjected to a cost-function minimization. Single hidden layer multilayer perceptron (MLP) networks trained with backpropagation algorithm are used in this work. More details of the MLP modeling approach can be found in [2, 3].

The proposed method uses a separate ANN for each element of the EC as shown in Fig. 1(b) to guarantee a continuous model with good accuracy. Once they promise good accuracy, all the ANNs (for I_D, C_{GD} and C_{GS}) are implemented in Verilog-A to realize the EC that can

predict the static and dynamic behavior of the device during circuit simulations.

4 Experimental results and discussion

First, I_D, C_{GDi} and C_{GSi} are obtained from the developed model at various bias voltages, from the Cadence Spectre circuit simulator. They show good agreement (<5 % mean absolute relative error) with the corresponding measurements, as it can be observed from Fig. 6.

Then this model is used to simulate the circuit, whose schematic and micrograph of the fabricated circuit (which is fabricated with the same conditions as the TFTs that are used to develop the model) with wire bonding are shown in Fig. 7. The resistor (R) is a discrete/external component to the circuit, allowing for increased flexibility during testing.

Small signal high-frequency model of the circuit is shown in Fig. 8. By applying KCL at node v_x,

$$\frac{v_x - v_{in}}{R} + sc_{gs1}v_x + sc_{gd1}(v_x - v_{out}) = 0$$
$$v_x = \frac{v_{in} + sRc_{gd1}v_{out}}{1 + sR(c_{gs1} + c_{gd1})} \quad (1)$$

similarly at node v_{out}:

$$sc_{gd1}(v_{out} - v_x) + g_{m1}v_x + \frac{v_{out}}{r_{o1}} + sc_{gs2}v_{out} + g_{m2}v_{out} + \frac{v_{out}}{r_{o2}} + sc_L v_{out} = 0 \quad (2)$$

(1) and (2) results in

$$A_v = \frac{v_{out}}{v_{in}} = \frac{g_{m1} - sc_{gd1}}{As^2 + Bs + C} = \frac{g_{m1} - sc_{gd1}}{(1 + \frac{\omega}{p1})(1 + \frac{\omega}{p2})} \quad (3)$$

where

$$A = R[c_{gd1}(c_{gs1} + c_{gs2} + c_L) + c_{gs1}(c_{gs2} + c_L)]$$
$$B = R[g_{m1}c_{gd1} + g_{m2t}(c_{gs1} + c_{gd1})] + c_{gd1} + c_{gs2} + c_L$$
$$C = g_{m2} + g_{ds1} + g_{ds2} \quad (4)$$

Therefore the circuit has two poles (p1 and p2) and a single zero ($\frac{g_{m1}}{2\pi c_{gd1}}$). When R is made to zero, the amplifier reduces to single pole system. In this case the amplifier gain (A_v) is given by

$$A_v = \frac{v_{out}}{v_{in}} = \frac{g_{m1} - sc_{gd1}}{s(c_{gd1} + c_{gs2} + c_L) + g_{m2} + g_{ds1} + g_{ds2}} \quad (5)$$

Therefore the pole is given by,

$$p1 = -\frac{g_{m2} + g_{ds1} + g_{ds2}}{2\pi(c_{gd1} + c_{gs2} + c_L)} \quad (6)$$

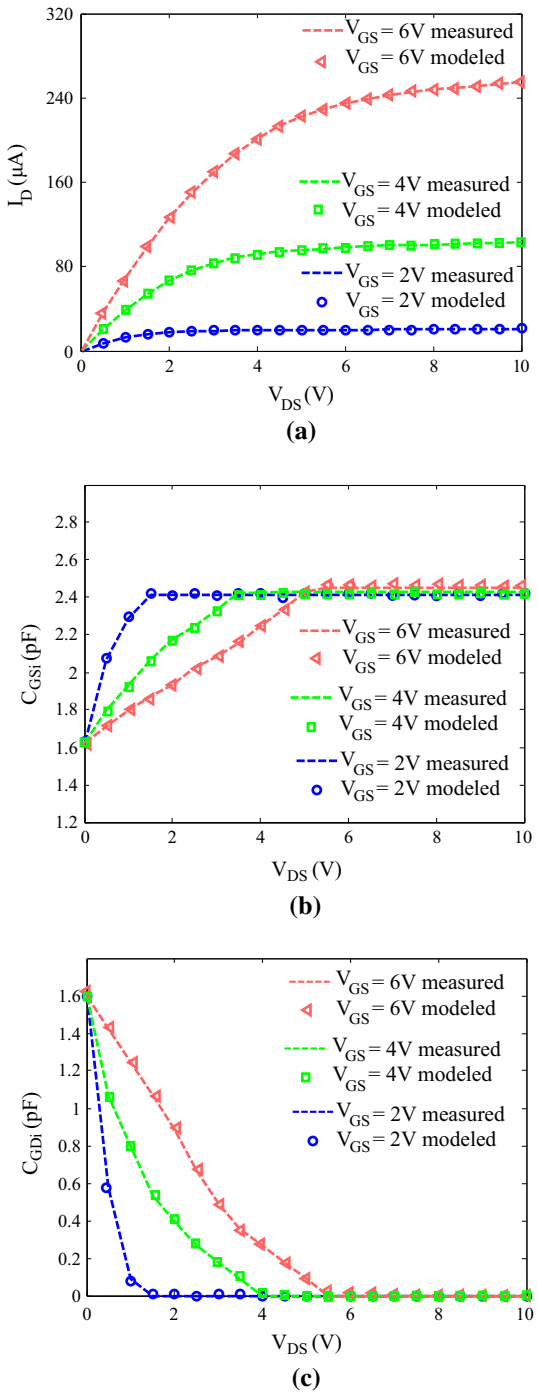

Fig. 6 Verilog-A neural model performance validation from the measurements $0 \leq V_{DS} \leq 10$ V in steps of 0.5 V and $2 \leq V_{GS} \leq 6$ V in steps of 2 V: **a** I_D. **b** C_{GSi}. **c** C_{GDi}

and the low frequency small signal gain is given by,

$$-\frac{g_{m1}}{g_{m2} + g_{ds1} + g_{ds2}} \quad (7)$$

This circuit simulations and measurements were carried out with a 4 pF load and a power supply (V_{DD}) of 6 V.

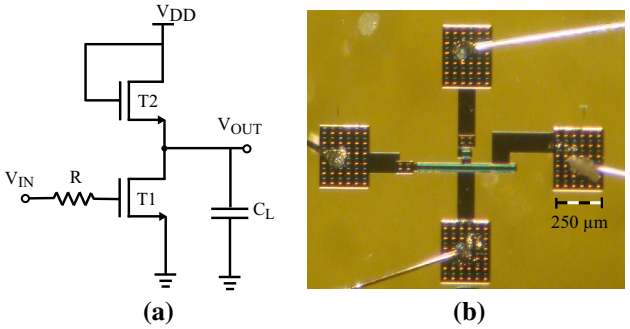

Fig. 7 CS amplifier **a** schematic—$W_{(T1)}$ = 640 µm and $W_{(T2)}$ = 40 µm. **b** Fabricated circuit micrograph after wire bonding

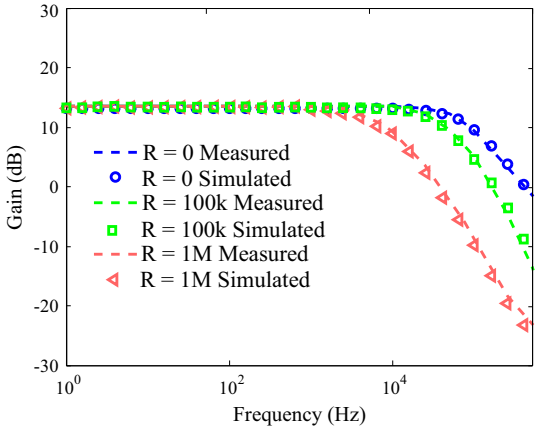

Fig. 9 CS amplifier frequency response

Measurements were performed under normal ambient at room temperature with the help of AFG3021B single channel arbitrary function generator and DS2024B four channel digital storage oscilloscope. Frequency response of the circuit is shown in Fig. 9 with different values of R (0 Ω, 100 KΩ and 1 MΩ). Corresponding dominant pole is presented for each case in Table 1, both from simulations and measurements, which is also well predicted by (3) and (4).

During amplifier characterization from measurements, care has been taken to keep all the TFTs in saturation. This amplifier resulted in 12.2 dB gain as predicted by (7). It also has shown a very low power consumption of 50 µW and 85 kHz 3-dB frequency. Then, the circuit is characterized without R, for a sinusoidal input signal with 100 kHz frequency. Figure 10 shows the output signal and error (difference between the simulation and measured output) signal, which is showing 2.5 % mean absolute relative error. Corresponding THD from simulation and measurements are 14 and 11.2 %, respectively.

Later, the same circuit is tested as a logic inverter. When the input voltage (V_N) is set to a low value, T1 is almost turned *off* and nearly no current flows through the device. Consequently, the output voltage (V_{OUT}) approaches to $V_{DD} - V_{TH}$, because of the diode connected load. As V_{IN} gets higher, the drain current increases thus the voltage drops across T2, which results in a lower V_{OUT}. Figure 11 shows the transient response to a input square wave for three different frequencies. In can be noticed that output

Table 1 Dominant pole locations

	Frequency (kHz)		
	R = 0	R = 100 K	R = 1 M
Simulation (EC)	84	44	7.5
Measurement	85	45	8

high level amplitude is $V_{DD} - V_{TH}$ (=4.65 V) and low level is ∼0.15 V. In addition, small peaks can be distinguished in the output waveform in instants of time where the input transitions occur, mainly visible with the high frequency (50 kHz) signal. This is caused by charge injection from the transistor gate capacitance. Both load and transistor capacitors are responsible for the rise and fall times. The load transistor possesses less current capability (higher equivalent resistance) while the driver transistor (T1) has much higher current driving capabilities (wider transistor), which justifies the much higher rise time than the fall time. Such is a consequence of a design that favours some gain ($\sqrt{\frac{W1}{W2}}$) in detriment of symmetric swings, as it can be noticed from Fig. 11.

In all the circuits measurements, as the load (4 pF) is a reasonable value compared to the device intrinsic capacitances, measurements can really elevate the proposed

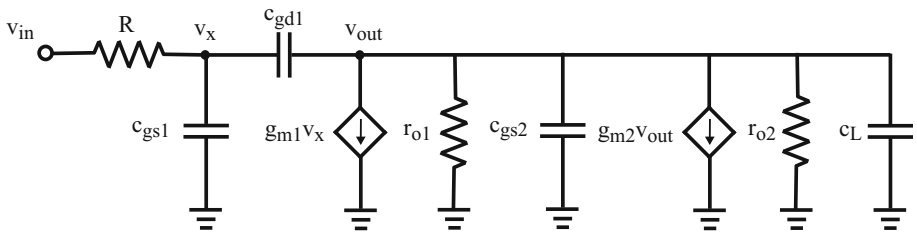

Fig. 8 small signal high frequency model of the CS amplifier including the load capacitor

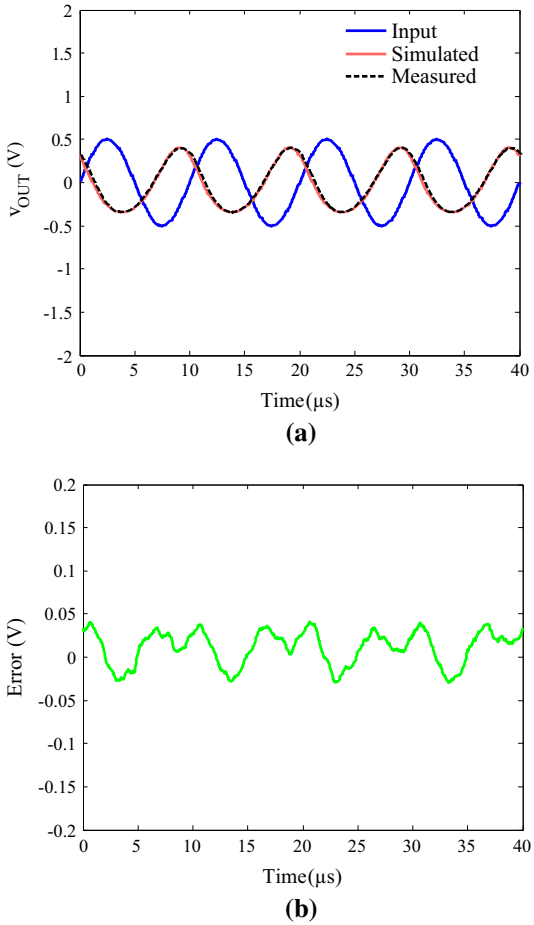

Fig. 10 CS amplifier response form simulations and measurements, when f is 100 kHz. **a** Output. **b** Error signal

model accuracy for both static and dynamic characterization. All the above results demonstrate the model ability to predict the small and large-signal behavior including non-linear effects of the parasitic capacitance from the circuit response. Circuit bandwidth can be improved by scaling down the devices (considering small lengths) and using self aligned structure (to minimize overlap capacitance).

5 Conclusions

This paper proposed an accurate behavioral model for the a-IGZO TFT using ANN based EC approach and implemented in Verilog-A for circuit simulations. Intrinsic capacitance of the device is characterized through measurements. Circuits simulations from the developed model have shown a good agreement with the corresponding measurements that demonstrates the modeling ability in predicting device static and dynamic behavior including non-linear distortion.

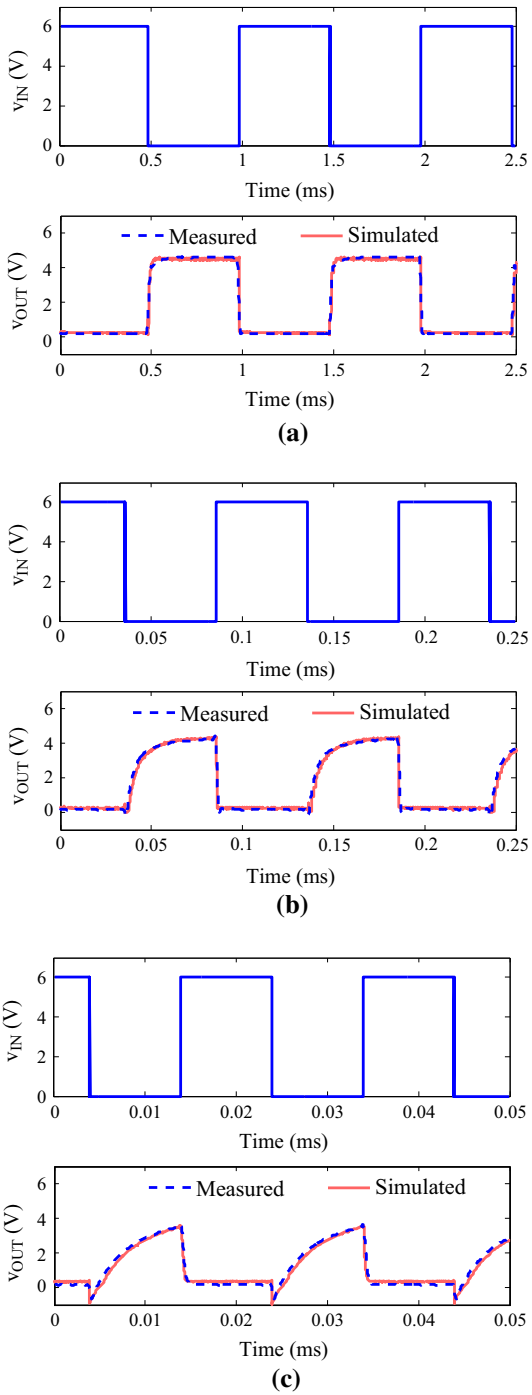

Fig. 11 Circuit transient response form simulations and measurements, when the input signal frequency is **a** 1 kHz. **b** 10 kHz. **c** 50 kHz

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30 invited lectures including 2 key-notes in international scientific conferences and workshops. His Figacurrent research focus is to take transparent electronics to performance and integration levels suitable for future ICTs. This involves pursuing reproducible and low temperature synthesis routes of high quality oxide nanostructures and integrating them in nanodevices and circuits, always complemented by device modeling/simulation.

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