Novel Linear Analog-Adder Using a-IGZO TFTs

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***Abstract*—A novel linear analog adder is proposed only with n-type enhancement IGZO TFTs that computes summation of four voltage signals. However, this design can be easily extended to perform summation of higher number of signals, just by adding a single TFT for each additional signal in the input block. The circuit needs few number of transistors, only a single power supply irrespective of the number of voltage signals to be added, and offers good accuracy over a reasonable range of input values. The circuit was fabricated on glass substrate with the annealing temperature not exceeding 200° C. The circuit performance is characterized from measurements under normal ambient at room temperature, with a power supply voltage of 12 V and a load of ≈ 4 pF. The designed circuit has shown a linearity error of 2.3% (until input signal peak to peak value is 2 V), a power consumption of 78 μW and a bandwidth of ≈115 kHz, under the worst case condition (when it is adding four signals with the same frequency). In this test setup, it has been noticed that the second harmonic is 32 dB below the fundamental frequency component. This circuit could offer an economic alternative to the conventional approaches, being an important contribution to increase the functionality of large area flexible electronics.**

***Index Terms*—Analog adder, IGZO TFTs, and linearization.**

I. Introduction

The attractive features of Indium-Gallium-Zinc-Oxide thin-film transistors (IGZO TFTs) are low-temperature fabrication, good optical transparency, relative high mobility [1], when compared to other TFT technologies, such as, a-Si:H and OTFT. Analog mixed-signal circuits with IGZO TFT technology [2], [3], [4] have already gained significant interest because of their potential applications in various fields [5], [6], [7].

The realization of analog adders is of considerable interest for most the linear analog circuits [8], neural networks [9], continuous time signal processing applications [10] and over-sampling data converters [11]. Though significant work was reported with CMOS technology [12], [13], [14], there was no attempt yet to realize it with IGZO TFTs. One of the possible reasons for this could be lack of stable and reproducible complementary (p-type) devices.

This paper presents a novel linear analog adder only with n-type IGZO TFTs. This design provides a simple way of adding 'n' number of signals to produce a single output without using any operational amplifier. Source degeneration technique is used to improve linearity performance of the circuit. In addition, care has been taken to compensate the gain loss from this linearization method, by using a simple output stage. This design used only a few number of TFTs and a single power supply.

Rest of the paper is organized as follows: Section II describes the device fabrication details. Section III presents circuit design and section IV explains the measured results. Finally, conclusions are drawn in section V.

II. Fabrication

The TFTs employed in the current work have a bottom-gate inverted staggered structure, being fabricated in Corning Eagle glass substrates. Gate electrode was e-beam evaporated and patterned by lift-off, consisting of 60 nm thick Ti/Au. A 250 nm thick dielectric following a multilayer approach consisting of SiO_2 + Ta_2O_5 + SiO_2 was then r.f. sputtered and patterned using reactive ion etching. This was followed by the deposition and lift-off patterning of r.f. sputtered IGZO layer, 40 nm thick. Source drain electrodes were processed with Ti/Au following similar procedure as described for gate electrode. Finally, devices/circuits were passivated with spin-coated SU8 transparent resist. Annealing in air at 200ºC for 1 hour was carried out prior passivation. In the designed circuit, all the TFTs have a channel length of 20 μm and a gate to source/drain overlap of 5 μm. These devices have shown a mobility of 17.4 cm^2/V·s, leakage current in the order of pA, and a turn-on voltage close to 0 V.

It has to be noted that the transparent devices and circuits can be achieved by employing transparent conductive oxides (e.g. IZO, ITO) as gate, source and drain electrodes and interconnects. However, this work used Ti/Au for source/drain as it can allow easy wire-bonding, which in turn facilitates flexibility in testing.

III. Circuit Design

The proposed circuit schematic and its micrograph before and after wire-bonding are presented in Fig. 1. This circuit is capable of adding an arbitrary number of signals. However, the fabricated circuit was designed to add up to four voltage signals. As it can be noticed from Fig. 1a, in order to enhance the ability of the circuit to add more number of voltage signals, a single TFT should be added in the input block (parallel to T1, T2 or Tn) for each additional signal without any other

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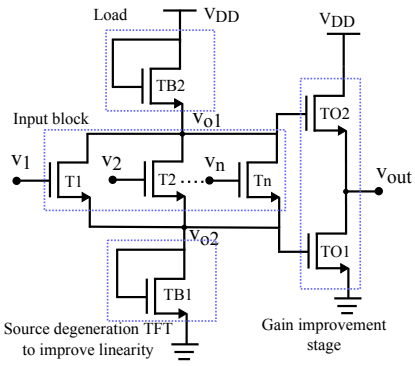
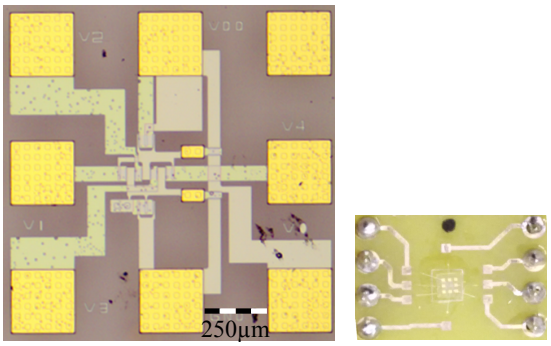
changes. It can be understood that the circuit does not impose limitations on the number of signals to be added.



(a)



(b)

Fig. 1. Novel adder: (a) Circuit schematic (b) Micrograph of the fabricated circuit and photo of wire bounded circuit.

In Fig. 1a, the diode connected TFT (TB1) acts as a source degeneration resistor with an equivalent impedance of $\frac{1}{g_{mB}}$, where g_{mB} is the transconductance of TB1. This TFT helps in improving the linearity performance of the circuit due to the negative voltage feedback. However, this imposes a limitation on the gain of the circuit, which is compensated by the output stage formed by TO1 and TO2.

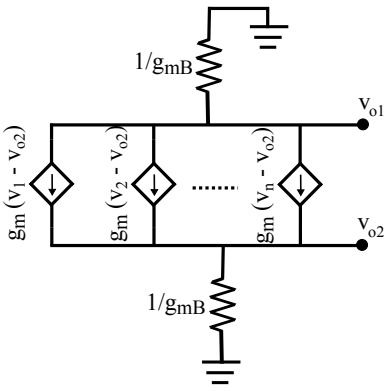


Fig. 2. Small signal equivalent of the circuit (excluding the output stage).

The small-signal equivalent circuit, formed by transistors T1 to Tn ,TB1 and TB2, is shown in Fig. 2. As the channel length of TFTs is relatively high, channel length modulation is ignored in the analysis. Assuming the same aspect ratios for all transistors, T1 to Tn, and under similar bias conditions, they will share the same small-signal transconductance value g_m, while the load and source degeneration transistors will be defined by g_{mB}. With the help of Fig. 2, the relationship between the output and input voltages can be derived as below,

$$\begin{aligned} v_{o1} &= -v_{o2} \\ v_{o2} &= \frac{1}{g_{mB}}\left[g_m(v_1 - v_{o2}) + g_m(v_2 - v_{o2}) + ... + g_m(v_n - v_{o2})\right] \\ v_o &= v_{o1} - v_{o2}, \quad \text{hence} \\ v_o &\propto -(v_1 + v_2 + ... + v_n) \end{aligned} \tag{1}$$

For the specific case, when $g_{mB} = ng_m$ i.e., $W_{(TB1/TB2)} = nW_{(T1,T2..Tn)}$, equation (1) can be reduced to

$$v_o = \frac{1}{n}\left[v_1 + v_2 + ... + v_n\right] \tag{2}$$

From (1), it can be noticed that this circuit can perform the summation of multiple signals. The average of the input signals can also be obtained as per (2).

IV. Results and Discussion

The circuit is characterized under normal ambient at room temperature. Circuit simulations were carried out with an in-house model. Measurements were taken with a power supply of 12 V and a load of approximately 4 pF (load is formed with an external unity gain buffer, whose frequency response is much higher than the measured range i.e., 1 MHz). Single channel arbitrary function generators (AFG3021B) and four channel digital storage oscilloscope (DS2024B) were used for the measurements.

The circuit is tested with the following stimulus.

$$\begin{aligned} v1 &= 5 + Asin(2\pi f_1 t), \\ v2 &= 5 + Asin(2\pi f_2 t), \\ v3 &= 5 + Asin(2\pi f_3 t), \\ v4 &= 5 + Asin(2\pi f_4 t). \end{aligned} \tag{3}$$

Its frequency response is presented in Fig. 3, when different number of input signals are applied to the adder. The circuit has shown approximately 115 kHz bandwidth and 78 μW power consumption, when all the input signals are applied.

The normalized measured response is compared and validated with the expected response as shown in Fig. 4, when f_1 = 250 Hz, f_2 = 500 Hz and f_3 = 1000 Hz and v4 is a constant bias. Ideal and measured linearity response of the circuit is presented in Fig. 5, when different number of input signals are applied. The circuit shows a linearity error $< 2.3\%$, until the input signal peak-to-peak value is 2 V. As expected,

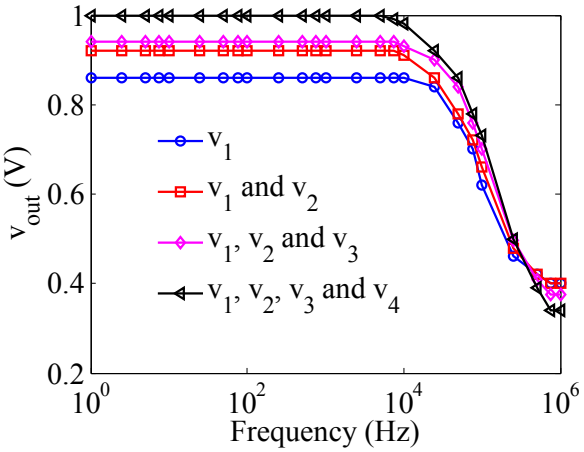


Fig. 3. Measured frequency response of the circuit with different number of input signals.

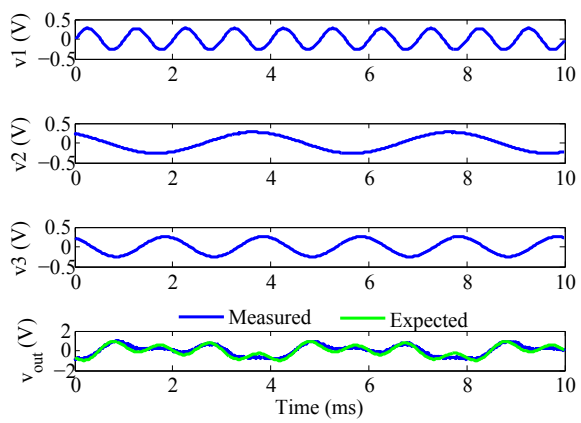


Fig. 4. Circuit characterization from measured and expected response in normalized form.

linearity error increases with respect to the increase in the input signal amplitude, which is due to the nonlinear behavior of the TFTs. The measured output signal (in inset) and its corresponding FFT are presented in Fig. 6 and 7, when the stimulus from equation (4) is applied, with all the signals have same frequency of 1 kHz, and a peak-to-peak amplitude of 2 V and 6 V, respectively. In case of Fig. 6, the second harmonic is 32 dB below the fundamental component, on the other hand, Fig. 7 shows high harmonic distortion (18 dB difference between the fundamental and second harmonic component) with increased input signal amplitude. Table I presents the difference between the fundamental and second harmonic components, when different number of input signals (amplitude 2 V peak-to-peak) are applied to the circuit. From these results it can be understood that the circuit shows minimum harmonic distortion for reasonable input signals amplitude.

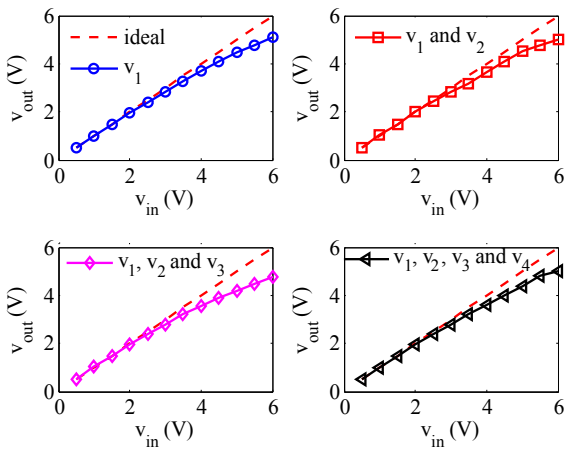


Fig. 5. Measured linearity response of the circuit with different number of input signals.

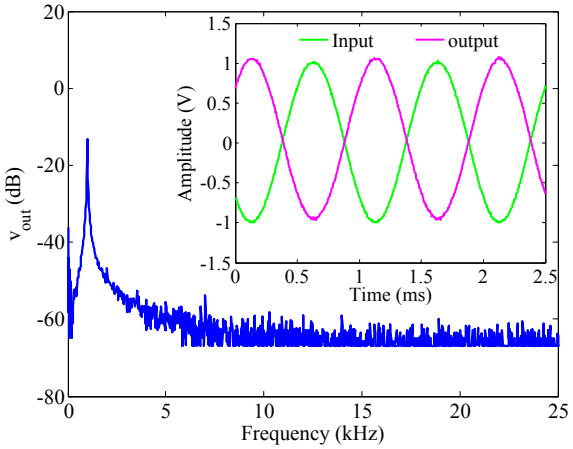


Fig. 6. Measured circuit response, when all the input signals peak to peak value is 2 V and frequency is 1 kHz.

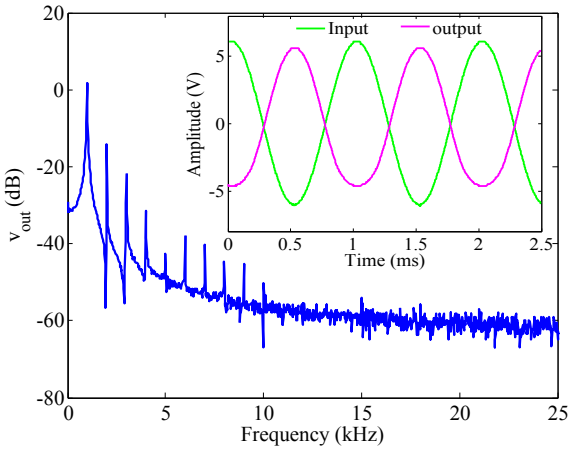


Fig. 7. Measured circuit response, when all the input signals peak to peak value is 6 V and frequency is 1 kHz.

TABLE I
DIFFERENCE BETWEEN FIRST AND SECOND HARMONIC LEVELS

No. of signals	Difference between first and second harmonic (dB)
1	42
2	36
3	35
4	32

V. CONCLUSIONS

For the first time a novel linear and low-power analog adder circuit with n-type IGZO TFTs is designed and characterized from the measurements, which was fabricated at low temperature (200°C). The proposed circuit does not need any operations amplifier. Further, the circuit has the ability to add up to four signals and the design can be easily extended for more number of input signals without any major changes. Linearity performance of the circuit was improved by using a simple source degeneration approach (using a diode connected transistor). Gain compensation was obtained with a simple output stage. From measurements, it was noticed that the linearity error is less that 2.3% up to the input signals with a peak-to-peak voltage values of 2 V, when adding four signals. Under the same testing condition, the circuit has shown a power consumption of 78 μW and a bandwidth of $\approx$115 kHz.

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