Transparent Current Mirrors With a-GIZO TFTs: Neural Modeling, Simulation and Fabrication

Pydi Ganga Bahubalindruni, Vítor Grade Tavares, Pedro Barquinha, Cândido Duarte, Pedro Guedes de Oliveira, Rodrigo Martins, and Elvira Fortunato

***Abstract*—This paper characterizes transparent current mirrors with n-type amorphous gallium–indium–zinc–oxide (a-GIZO) thin-film transistors (TFTs). Two-TFT current mirrors with different mirroring ratios and a cascode topology are considered. A neural model is developed based on the measured data of the TFTs and is implemented in Verilog-A; then it is used to simulate the circuits with Cadence Virtuoso Spectre simulator. The simulation outcomes are validated with the fabricated circuit response. These results show that the neural network can model TFT accurately, as well as the current mirroring ability of the TFTs.**

***Index Terms*—Transparent current mirrors, amorphous gallium–indium–zinc–oxide thin-film transistor (a-GIZO TFT), neural modeling.**

I. Introduction

AMORPHOUS gallium–indium–zinc–oxide (a-GIZO) thin-film transistor (TFT) technology has potential industrial applications in large-area, low-cost transparent display technologies such as AMOLED [1] and ultra definition LCD [2]. Fabrication can be achieved at low temperature, followed by heat treatment not exceeding 200°C. Furthermore, the high electrical mobility 20 $cm^2/V{\cdot}s$ [3] compared to other TFTs (a-Si:H : 1 $cm^2/V{\cdot}s$ [4], organic TFT : 0.1-–1 $cm^2/V{\cdot}s$ [5]), make a-GIZO TFTs attractive for transparent and flexible electronics [6]. These are the motivating factors to build analog circuits for various types of sensing and display applications, which will be portable and economic, resulting in integrated circuits that avoid interfacing problems. The analog circuit design is limited due to the lack of stable p-type TFT and unavailability of built-in libraries for the active and passive components. Nevertheless, few circuits are reported, mostly with depletion type TFTs such as a shift register [7] and a 6-bit current-steering DAC [8].

In order to design and simulate circuits, punctilious device models are necessary to predict the device behavior during simulations. Models based on device physics are generally used for circuit design. Nevertheless, physical models are complex and time consuming to develop. Especially physical modeling is not a good choice for novel technologies, such as a-GIZO, which are not yet well matured, and where experiments are still going on to ensure better behavior, either by changing device structure [9], materials for electrodes or processing conditions. All these factors certainly impact the density of states and charge carrier flow in the device. Whenever there is a change in any of the aforementioned factors, the corresponding device physics need to be studied and a new model needs to be developed. Possible alternative methods are table-based and neural network models that are built from the device measured characteristics. However, accurate table-based models [10] demand huge memory. Artificial Neural Network (ANN) modeling overcomes all these drawbacks without compromising performance. When quicker circuit design is important, with new devices as a-GIZO TFT, a simple, accurate and continuous model, with less development time is desired. ANNs have all these properties, and in fact, multilayer feedforward network has already been successfully applied to model MOSFETs, as proposed in [11]. The current work includes the complete device behavior, i.e., intrinsic and extrinsic, by taking the series resistance (R_s+R_d) of source and drain electrodes into account. If only the intrinsic behavior of the device needs to be modeled, the impact of $R_s + R_d$ should be deembeded from the measured data. Then, the network needs to be trained with this new data. The extraction method of R_s+R_d should basically follow the same procedure as in physical modeling. General steps in physical and ANN based modeling approaches are shown in Fig. 1.

Current mirrors are important functional blocks in analog circuit design, which find applications in providing bias, as an active load and pixel driving circuits in OLED displays [12]. ZTO TFT-based current mirrors have been already reported in the past, but with metallic electrodes and requiring a high post-processing temperature of 400 °C [13]. In this work we are reporting simple current mirrors with two TFTs having different mirroring ratios and a cascode mirror, all based on fully transparent GIZO-TFTs with processing temperatures not exceeding 200 °C. As a first step, an ANN model is developed from the measured data of the TFTs, being then implemented in Verilog-A for circuit simulation using Cadence Virtuoso Spectre.

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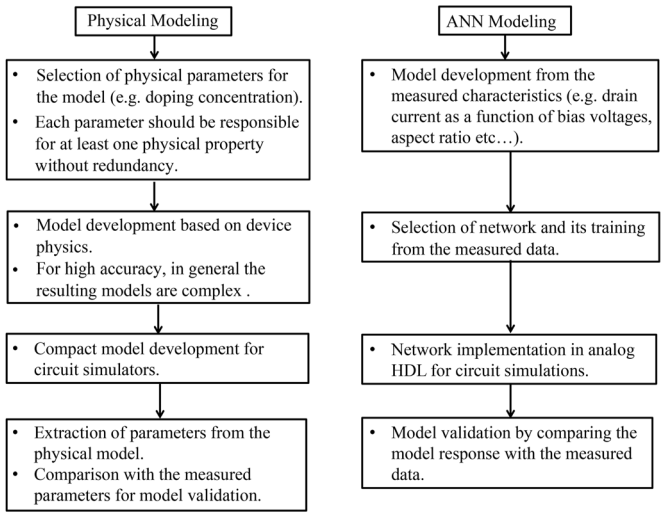

Fig. 1. General steps in physical and ANN based modeling methods.

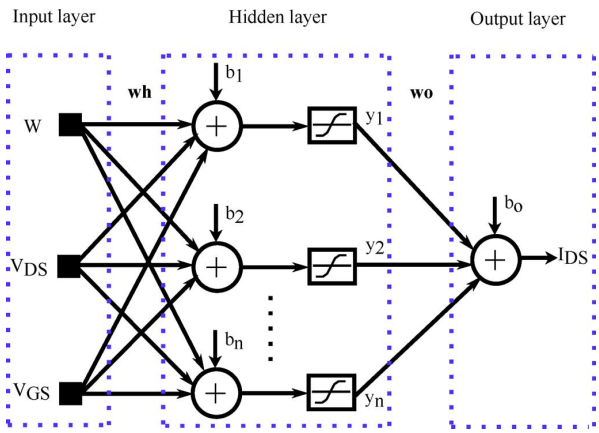

Fig. 2. Topology of the feedforward ANN model with a single hidden layer.

Finally, circuits are fabricated. A comparison of simulated, fabricated circuits and the expected results are presented to demonstrate the ANN modeling ability, as well as current mirroring capability of the a-GIZO TFTs.

II. Neural Modeling

A multilayer feedforward network, with a single hidden layer and a sufficient number of neurons, is a universal approximator [14]. This is the minimum structure adopted in this work to minimize complexity, with the typical single-hidden layer topology as shown in Fig. 2. Backpropagation algorithm is used for training. The network learns the function that needs to be approximated from the training data (i.e., I_{DS} as a function of W, V_{DS} and $\mathrm{V_{GS}}$). The hidden layer neurons perform weighted summation followed by a limiting function, whereas the output neuron only performs a weighted summation (linear neuron). During the training phase, the network calculates the output from the given inputs in the forward direction. This is compared to the expected value and the error is propagated in the backward direction, which in turn modifies the weights and biases of the network to minimize the error. The network stops learning at a point when the validation error starts increasing.

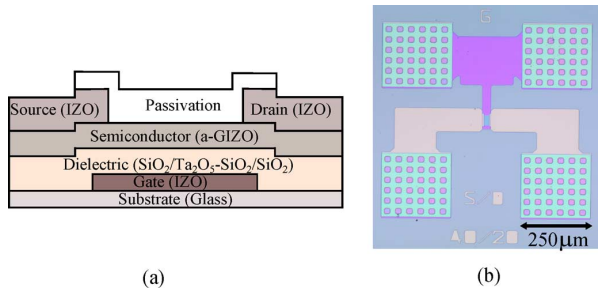

Fig. 3. Transparent a-GIZO TFTs: (a) Schematic of the device cross section, with a staggered bottom gate configuration (b) Micrograph of one isolated device, with $\mathrm{W/L} = 40/20\ \mu\mathrm{m}$.

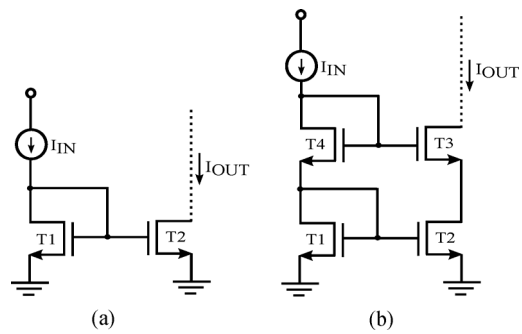

Fig. 4. Current mirrors schematics. (a) With two-TFTs. (b) Cascode.

Validation data is a portion of the input data that is not used to train the network, but just to verify the performance during training.

III. Circuit Design and Fabrication

A Schematic of the cross-section and a micrograph of the fabricated transparent oxide TFTs are shown in Fig. 3. TFTs and circuits (integrated in the same 2.5×2.5 cm^2 glass substrates) were fabricated with a staggered bottom gate structure and annealed at 200 °C. Gate, source and drain electrodes are based on $\mathrm{In_2O_3}$-ZnO (IZO, 200 nm thick), the oxide semiconductor is $\mathrm{Ga_2O_3}$-$\mathrm{In_2O_3}$-ZnO (GIZO, 30 nm thick) and the dielectric layer is a multicomponent/multilayer structure composed of $\mathrm{SiO_2/Ta_2O_5\text{-}SiO_2/SiO_2}$, 350 nm thick. All these layers were deposited by RF magnetron sputtering without intentional substrate heating, using a home-made system (IZO) and an AJA ATC-1300F system (GIZO and dielectrics) [15]. The electrodes and the semiconductor were patterned using a lift-off process, while the dielectric was etched by reactive ion etching. More details regarding the processing and properties of these thin films and devices can be found in [16], [17]. On the top of this structure, a SU8 layer was spin-coated to act as a passivation layer, being patterned using conventional UV exposure and development processes [18].

Schematics of two-TFT and cascode current mirrors are shown in Fig. 4(a) and (b) respectively. The two-TFT current mirrors micrographs of the fabricated circuits with different mirroring ratios are shown in Fig. 5. Different widths ($W = 40\ \mu$m, 80 μm, and 320 μm) have been used for the transistor T2 to obtain different mirroring ratios, with all the TFTs

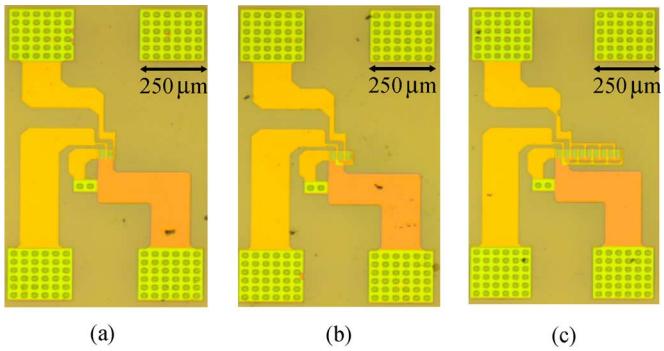

Fig. 5. Micrographs of transparent two-TFT current mirrors based on a-GIZO TFTs. (a) $(.W)_{T2} = 40\ \mu$m. (b) $(W)_{T2} = 80\ \mu$m. (c) $(W)_{T2} = 320\ \mu$m.

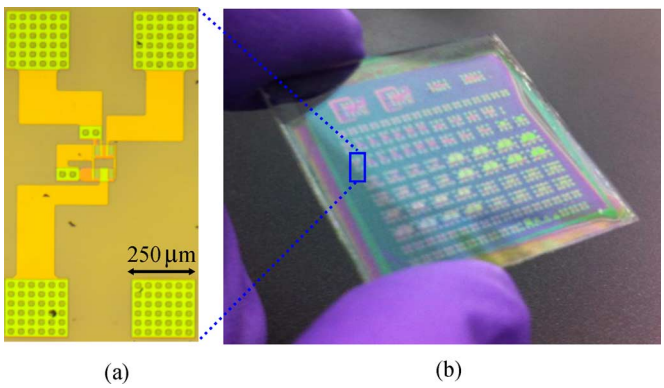

Fig. 6. (a) Micrograph of the transparent cascode current mirror based on a-GIZO TFTs with $W/L = 40/20\ \mu$m for all the TFTs. (b) Entire glass substrate with circuits and isolated devices.

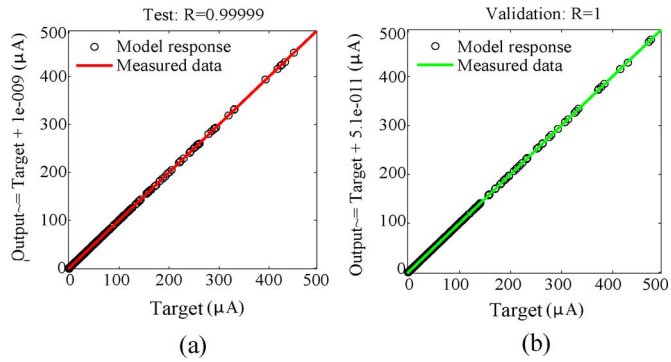

Fig. 7. ANN modeling response for a-GIZO TFTs. (a) Testing data performance. (b) Validation data performance.

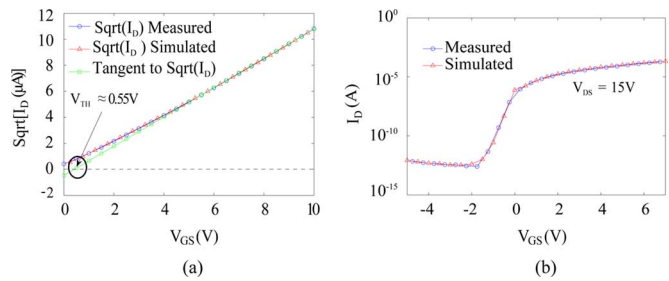

Fig. 8. (a) Threshold voltage (V_T) calculation from the measured and simulated data (using the Verilog-A model—example with the 80 μm TFT). (b) Measured and modeled transfer characteristics of transistor whose width is 320 μm.

having a channel length (L) of 20 μm. The cascode current mirror fabricated circuit is shown in Fig. 6(a). In this circuit, all TFTs (T1 to T4) have the same width (40 μm). A photo of the glass substrate containing all the mentioned circuits, as well as isolated devices (TFTs), is shown in Fig. 6(b).

IV. Results and Discussion

In order to develop the ANN model, measured data (averaged from two similar devices in two similar chips) are taken from the fabricated TFTs. The measurements have been performed using a semiconductor parameter analyzer Keithley 4200-SCS, and a Cascade Microtech M150 probe station under darkroom conditions. Matlab is used to train the network. The input data to the ANN is randomly divided into training (60%), validation (20%) and testing (20%). From the training data, the ANN learns the function that needs to be approximated. Validation data is used for stopping criteria, which ensures no over-fitting during the training phase. In its turn, testing data (never seen during training) are used to evaluate the generalization ability of the network. In the current case, a single hidden layer network with 25 neurons presented a good performance. Post-training values for testing and validation data are shown in Fig. 7(a) and (b) respectively. These results show good agreement between the measured data and modeled response as the regression factor (R) is almost one. The resulting network is implemented in Verilog-A and it is used for all the aforementioned circuit simulations with Cadence Spectre simulator. The threshold voltages (V_T) of the TFTs can be calculated either from the simulated data using the developed Verilog-A model or from the measured data as shown in Fig. 8(a). Fig. 8(b) demonstrates very good agreement between measured and simulated transfer characteristics of a TFT at $V_{\rm DS}$ 15 V, where the TFT width is 320 μm, reinforcing the validity of the model in the complete region of operation. However, a separate network has been used to model the region for $V_{\rm GS} \leq 0$ V, as the current in the cut-off region spreads over several orders of magnitude. Nevertheless, one should note that the model is built with the intention of designing analog circuits, where generally, $V_{\rm GS} \geq 0$ V.

For the current mirror circuits, ignoring channel-length modulation (λ) due to long length of the devices and assuming that they are matched, the relation between input $(I_{\rm IN})$ and mirrored $(I_{\rm OUT})$ current can be expressed (for both topologies) as

$$\frac{I_{\rm OUT}}{I_{\rm IN}} = \frac{W2(V_{\rm GS} - V_{T2})^2(1 + \lambda V_{DS2})}{W1(V_{\rm GS} - V_{T1})^2(1 + \lambda V_{DS1})} \approx \frac{W2}{W1} \qquad (1)$$

where V_{T1} and V_{T2} are the threshold voltages of the transistors T1 and T2, respectively. Fig. 9 shows the results for the two-TFT current mirrors with different mirroring ratios: simulation, expected, and measured responses are plotted (with mismatch removed by offsetting the simulation current). Similar re-

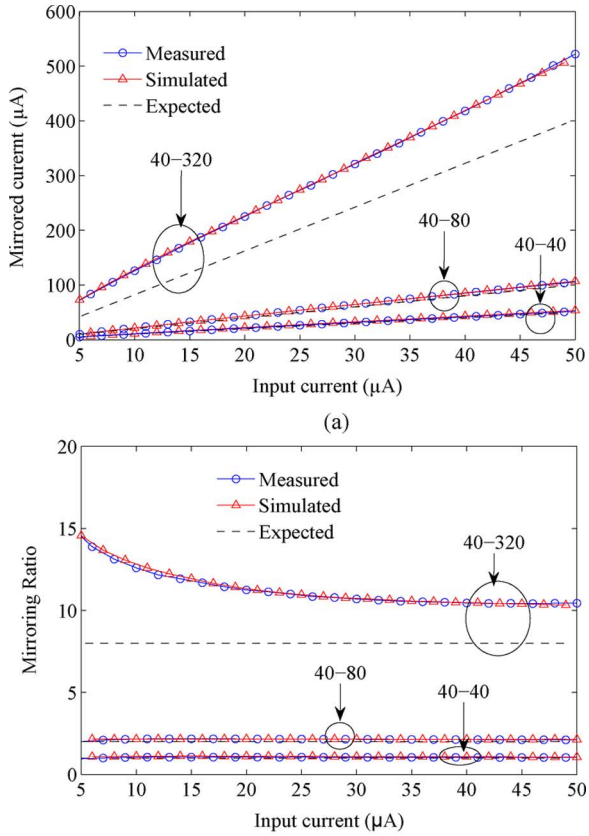

Fig. 9. Two-TFT current mirror response: expected, from neural model simulation and measured response with fabricated circuits. (a) Mirrored current. (b) Mirroring ratios.

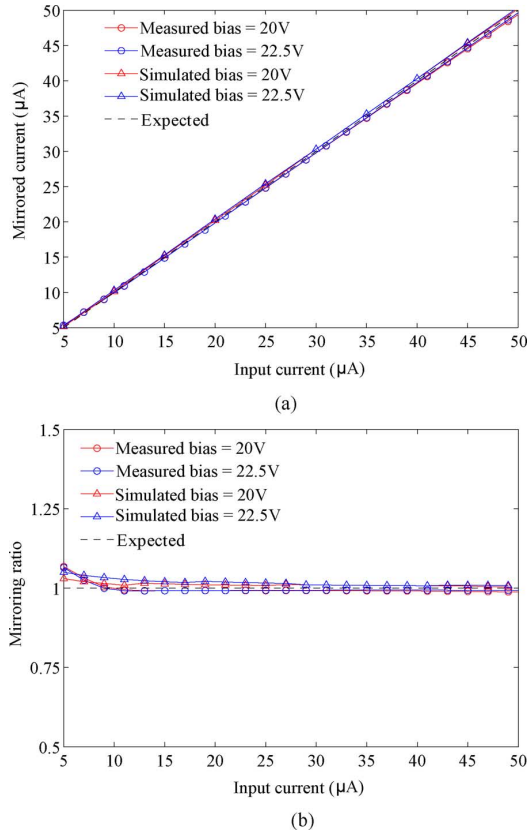

Fig. 10. Cascode current mirror response at different bias voltages: expected, from neural model simulation and measured response with fabricated circuits. (a) Mirrored current. (b) Mirroring ratios.

TABLE I
MIRRORING RATIOS

Mirrors	40-40	40-80	40-320	Cas (20V)	Cas (22.5V)
Expected	1	2	8	1	1
Simulated	1.093	2.149	11.43	1.011	1.017
Measured	1.041	2.135	11.7	0.997	0.997

sults for the cascode current mirror, at different bias voltages, are shown in Fig. 10.

The average mirroring ratios of all the current mirrors are listed in Table I. Results show good agreement between the metrics (expected, simulated and measured) at lower mirroring ratios, whereas at higher mirroring ratio, there is a higher mirrored current, which is related to the fingered layout of output the transistor that tends to have a lower threshold-voltage. Nevertheless, the simulation results capture the non-ideal behavior properly. For the 40–320 current mirror, the negative slope in Fig. 9(b) is caused by a threshold-voltage mismatch between the input and output transistors.

V. CONCLUSION

Current mirror circuits based on fully transparent a-GIZO TFTs annealed at 200 °C are demonstrated. A neural model is developed from the measured data of the TFTs and implemented in Verilog-A. This model's response is in good agreement with the measured data. Circuits have been simulated with the developed model using Cadence Spectre simulator. When the simulation results are compared to the fabricated circuits' response, they reveal a good degree of prediction capability for the actual transistor behavior within the circuit operation.

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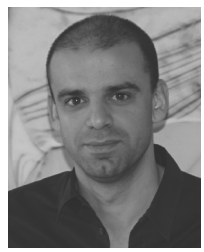

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