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Filter & hold: a mixed continuous-/discrete-time technique for time-constant scaling

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SUMMARY

The work reported in this paper introduces a periodic switching technique applied to continuous-time filters, whose outcome is an equivalent filter with scaled time-constants. The principle behind the method is based on a procedure that extends the integration time by periodically interrupting the normal integration of the filter. The net result is an up scaling of the time constant, inversely proportional to the switching duty-cycle. This is particularly suitable for reducing the area occupied by passive devices in integrated circuits, as well as to accurately calibrate the filter dynamics. Previous works have been following this concept in an entirely continuous-time perspective, either focusing on specific circuits or using approximations to provide an extended analysis. This paper includes input/output sampling to derive a closed-form representation for the scaling technique herein coined as 'Filter & Hold' (F&H). A detailed mathematical analysis is described, demonstrating that the F&H concept represents an exact filtering solution. Simulation results and experimental measurements are provided to further validate the theoretical analysis for an F&H vector-filter prototype. Copyright © 2014 John Wiley & Sons, Ltd.

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KEY WORDS: continuous-time filters; discrete-time filters; time-constant scaling; tunable filters

1. INTRODUCTION

The persistent miniaturization driven by downscaling in silicon processes has enabled a variety of fast digital devices and circuits. Although an elementary switch can be further implemented within reduced sizes, other circuit components, such as resistors and capacitors, do not scale accordingly. Consequently, certain applications relying on passive devices are severely constrained in terms of area and power consumption. This is the case of most filter circuits in which the passive devices play a crucial role defining large time-constants. In typical continuous-time realizations of analog filters, the cut-off frequencies are in the order of tens of kilohertz. However, some applications require much lower bandwidths, around tens to hundreds of hertz. Hence, additional parametric scaling techniques are demanded as reduced cost alternatives to off-chip capacitors with large values. Capacitor multipliers [1], current scaling [2] or very-high active resistor implementations [3] are different solutions that have been frequently employed in electronic systems for biology, in order to comply with the needed long time-constants. However, these or other filters, even if purposely designed for low sensitivity to RC time constants [4], when integrated in CMOS, accuracy and flexibility for calibration are in general necessary to compensate for process and temperature

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variations [5–10]. For G_m-C filters, this generally involves digital-to-analog interfaces wherein fine-resolution control is simultaneously correlated with increased area and power. For discrete-time processing, switched-capacitor (SC) and switched-current (SI) are the preferred filtering techniques. The former provides high-precision time-constants while the latter is suitable for standard technologies [11]. Nevertheless, for systems with repeated similar blocks, neither technique is area efficient. This paper addresses a mixed-time technique that, in essence, is a continuous-time system with integration switching. The technique, herein referred to as 'Filter and Hold' (F&H), can accomplish very large time-constants from smaller values of reference. The term F&H derives from the fact that the 'filter' (or linear dynamical system) will be allowed to operate as a normal continuous time filter for a given small period of time. Then the integration is halted and the last state is 'hold' for another period of time.

The effect of periodically switching RC networks, as a way to obtain larger time constants, has actually been studied in the late sixties [12–14]. Sun and Frisch presented in [13] a mathematical approach based on state-space analysis to describe this effect on a generic passive RC network. However, the basic behavior was validated assuming filter bandwidths much lower than the switching frequency, which allowed for a linear approximation of the exponential matrix. Other works followed the same assumption, but using different approaches. Kaehler presented a mathematical analysis based on differential equations [14], while Bruton and Pederson used the impulse response of an RC network at a capacitance node [15]. The concept was further extended later as 'switched-resistors' circuits [16–18].

Switching at a given duty-cycle, to scale time, finds usefulness in a wide range of applications [17,19–24]. Tsividis and Vallancourt works, developed during the eighties [19–21], proposed a synthesis procedure for generic filters based on programmable delay blocks (z^{-1}) built from an analog integrator similar to an RC network. More recently Xiao *et al.* [23] have presented an R-MOSFET-C filter with corner frequency controllable by the switching duty-ratio. The advantage of this methodology has been further demonstrated through CMOS implementations for low-voltage and high-linearity operation [17,24].

In the present work, the F&H synthesis starts from a continuous-time filter prototype. Based on a continuous- and discrete-time approach, an effective generalization of the periodically switching operation is possible for different types of filters and for all classes (low-pass, high-pass, band-pass and band-reject) without aliasing effect under input band-limited signal assumption. Most importantly, it is shown that the F&H technique represents an exact filtering solution, which is very different from what has been reported in literature so far for similar techniques that are based on continuous-time filter prototypes. The implementations are constricted to band-limited transfer functions (low-pass and band-pass), where the original poles of the system need to be kept in frequencies much lower than the sampling frequency [15].

This paper is organized as follows. First, the F&H concept is described along with an illustrative example, and then the generality of the technique is presented in detail. Active filter simulations are presented in Section 3, with experimental results from measurements included in Section 4.

2. THE F&H DISCRETE-TIME FILTER

Circuits function by controlling electrical variables (currents and voltages) in time. Necessarily, there must be only one way to increase the apparent value of passive elements that somehow dictate the dynamical behavior of a system, presumably considered linear in the present context. Confining the analysis to active systems where resistors and capacitors govern dynamics, the resulting time-constants can be virtually increased through scaling of electrical variables (typically the capacitor current) by either direct scaling [26] or by compressing or expanding the time reference during integration of the electric variables. The F&H technique follows this last approach by effectively setting different time scales in circuit operation. The integration time of the system is made longer by 'freezing' the time in a given interval that is periodically repeated. From the standpoint of the time reference (defined by a clock signal), the response will then appear as if materialized in a system with long dynamics, although the physical elements in the circuit may in fact describe a faster system.

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2.1. Concept

For the sake of simplicity, let us initially consider a first-order passive filter shown in Figure 1. If the switch is always closed, the topology can easily be identified as a first-order high-pass filter. The inputs and outputs of the RC circuit are always assumed sampled-and-held according to the time-reference clock in Figure 2. The switching is performed such that the current is allowed to flow through the capacitor during a brief period of time α controlled by the clock signal ϕ_1. For the remaining time period, $T-\alpha$, this current is zeroed. The signal clock ϕ_2 controls the moment when the input and output of the filter are sampled, setting by definition an equivalent discrete-time system between both outputs of the sample-and-hold (S&H). These signals are then held constant and equal to the values sampled at any given normalized sampling-time n, until the next clock cycle. The pulse duration of ϕ_2 is important to comply with the real S&H dynamics, but for the interest of demonstration, the duration is not a significant factor if the S&H is considered ideal. However, it should be noted that it is fundamental to keep both clock cycles non-overlapped to decouple input signal changes with the filter integration.

When the clock ϕ_1 turns to *on* state, at $t=(n-1/2)T-\alpha$, the voltage at the input of the RC circuit is already fixed to a value $v_i[(n-1)T]$ set by the S&H, as previously referred. If the capacitor holds some initial voltage, i.e. $v_C=v_i[(n-2)T]-v_o[(n-1)T]$, then the difference equation of the system can be found by the step response

$$v_o[nT]=\{v_o[(n-1)T]+v_i[(n-1)T]-v_i[(n-2)T]\}\cdot \mathrm{e}^{-\alpha/(RC)} \tag{1}$$

The respective z-transform can be defined as follows

$$\frac{V_o(z)}{V_i(z)}=\frac{1-z^{-1}}{1-e^{-kT/(RC)}\cdot z^{-1}}\cdot z^{-1}\cdot \mathrm{e}^{-kT/(RC)} \tag{2}$$

where $k=\alpha/T$ represents the duty-cycle of ϕ_1. The filter represented by (2) is indeed high-pass, with a zero at $z=1$ as anticipated for a high-pass filter, and a pole at $z=e^{-kT/(RC)}$. Changing neither the time

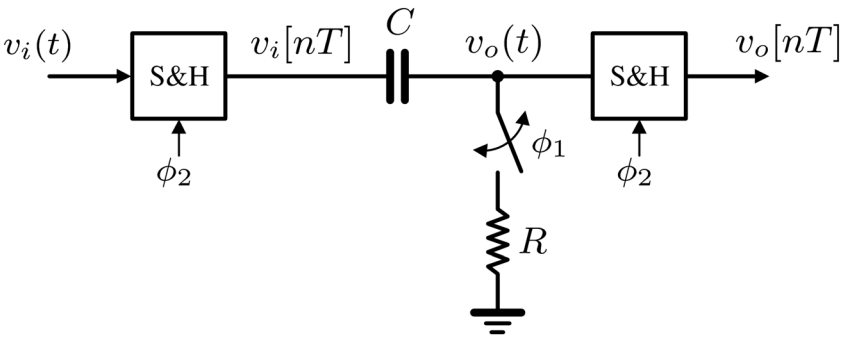

Figure 1. Illustration of the F&H concept in a high-pass filter.

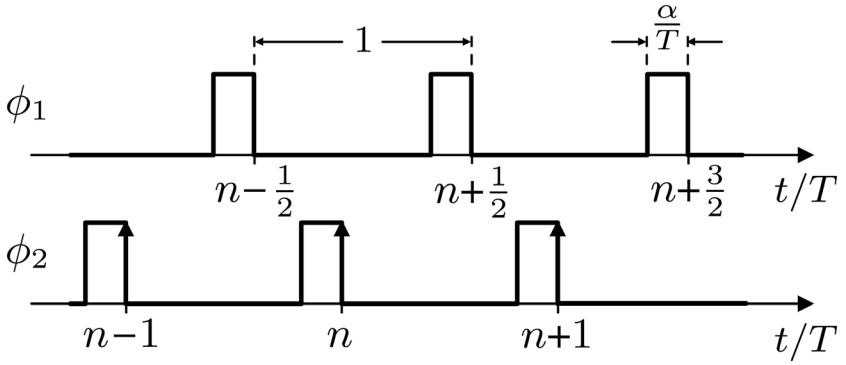

Figure 2. F&H sampling signals.

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period T nor RC, solely depending on the value of k, this pole can be made close to $z=1$. However, if k is kept constant (as well as RC), changing T does not modify the pole position in relation to the input signal bandwidth. The relative decrease or increase of pole position is followed by the same amount of relative input bandwidth compression or expansion in terms of the normalized frequency $|\omega|=|T\cdot\Omega|<\pi$ (where Ω represents the frequency of the continuous-time processing). The sampling period changes both input sampling and system bandwidths. This is an interesting property that is not followed by SI or SC circuits. The pole and zero positions depend only on transistor (SI) and capacitor ratios (SC). A different sampling frequency will change only the relative signal bandwidth in the normalized frequency spectrum, but the filter pole and zero positions are kept unchanged. Consequently, adjusting the sampling period in an SC and SI filter affects the filtered signal, as it also affects the signal time resolution. In opposition, F&H signal resolution and filtering characteristic can be decoupled. As $k/(RC)$ is kept constant, changing T changes the resolution of the signals, but the pole and zero positions of the filter, relatively to the input signal bandwidth, are preserved. If, however, a change in the filter characteristic is needed, just adjust k.

Figure 3 shows a simulation result for the high-pass F&H circuit shown in Figure 1, together with the continuous-time prototype response (for the same sample-and-held signal). The transient analysis was performed in Cadence Spectre simulator, with ideal components and S&H circuit models, both at input and output of the filters. The resistor and capacitor were set to $R=10\,\text{k}\Omega$ and $C=1\,\text{nF}$, respectively, and the duty-cycle is $k=0.1$. The capacitor is set to a ten times bigger value, $C=10\,\text{nF}$, for the continuous-time prototype. As expected, the response of the F&H is the same as the RC continuous-time filter, except that the output is sampled and delayed. Figure 3 also shows a zoom in of a squared area for better understanding. With the same duty-cycle, the simulation shows that the filter behavior is not affected by the sampling period, only the time resolution changes. Another interesting detail, and the actual main useful feature, is parameter scaling. As referred earlier, the time constant is scaled by k. Given that k is less than one, a $k\cdot C$ smaller capacitor can be used to achieve an equivalent time constant $\tau=R\cdot C$.

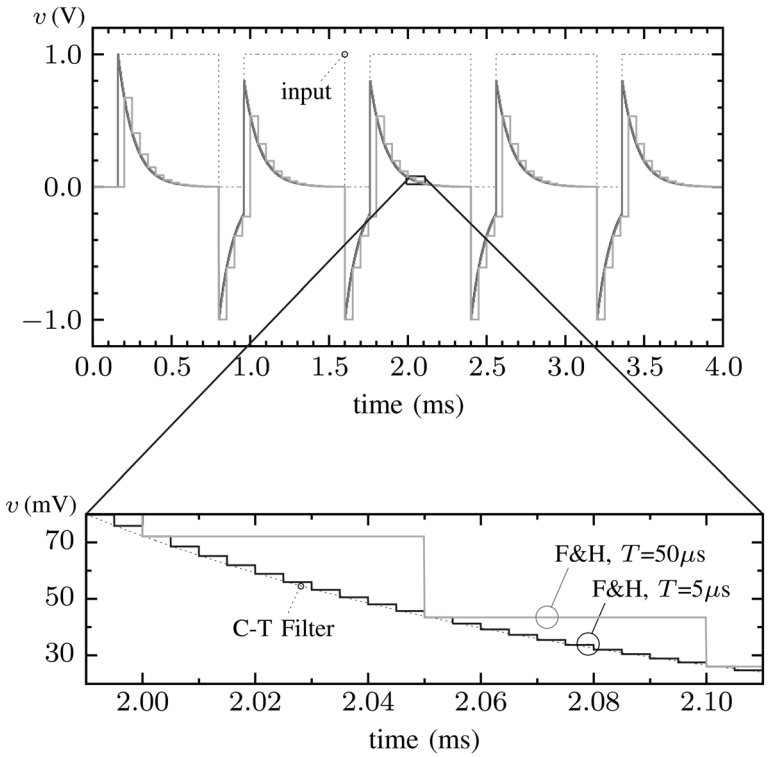

Figure 3. Two high-pass F&H results (duty-cycle of 0.1 in both) over the same input signal against the continuous-time (C-T) filter response. A zoomed time frame is also shown.

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2.2. Generality

Finding out whether other filter topologies can be implemented with an F&H and on what terms can be applied are questions that have to be addressed from a general standpoint. To get the required answers, the following demonstrations will always assume that the input (and output) is sampled-and-held, a key property in the overall F&H concept that allows a depart from a 'hybrid' — continuous/discrete time system — to a full discrete-time system with closed form representation. This is a very distinct feature that makes the approach general and not solely confined to band-limited type of transfer functions (low-pass or band-pass) as commonly found in literature. Let us then start by assuming a band-limited input signal $u(t)$ applied to a sample-and-hold circuit considered ideal and perfectly buffered at input and output. In fact, any nonlinear contribution from the S&H will just affect the sampled input that now presents more harmonics. So, if this needs to be considered, the following derivation is still perfectly valid, but now the input just needs to include the generated harmonics. Then, ideally, the resulting sampled signal $u_s(t)$ can then be expressed as

$$u_s(t) = \mathrm{rect}\left(\frac{t - T/2}{T}\right) \cdot \sum_{n=-\infty}^{+\infty} u(t) * \delta(t - nT) = \sum_{n=-\infty}^{+\infty} u_n \cdot \mathrm{rect}\left(\frac{t - nT - T/2}{T}\right) \tag{3}$$

where $u_n = u[nT]$, T is the sampling period, '*' is the convolution operator, $\delta(t)$ a Dirac function and rect(·) is the pulse function given by

$$\mathrm{rect}\left(\frac{t - T/2}{T}\right) \equiv \begin{cases} 1, & 0 \le \mathrm{t} < T \\ 0, & \textit{otherwise} \end{cases} \tag{4}$$

The sample-and-held signal $u_s(t)$ is applied to a linear continuous-time system described by a state-space model, in the general form

$$\dot{\boldsymbol{x}}(t) = A\, x(t) + \mathrm{B}\, u_s(t) \tag{5a}$$

$$\boldsymbol{y}(t) = C\, x(t) + \mathrm{D}\, u_s(t) \tag{5b}$$

where $A \in \mathfrak{R}^{m \times m}$, $B \in \mathfrak{R}^{m \times 1}$, $C \in \mathfrak{R}^{1 \times m}$ and $D \in \mathfrak{R}$. Before going any further, it is important at this point to give some physical meaning to the model represented in (5). The F&H presented in the previous example relied on switching the current that charges (or discharges) a capacitor. The same method needs to be applied to the state-space representation herein described. In an active filter, the state variables are associated with capacitor voltages, defined as $\dot{v}(t) = dv(t)/dt = i(t)/C$. If the system dynamics is solely determined by capacitor and resistor-like elements, then $\dot{\boldsymbol{x}}(t)$ represents a vector voltage derivative and the right-hand side of (5a) represents a current vector flowing through the capacitors. In order to make (5) an F&H representation, the integration just needs to be halted every T seconds for a time duration of $T - \alpha$ seconds. Therefore, its formal representation can be defined by

$$\dot{\boldsymbol{x}}_{\mathrm{FH}}(t) = (A\, x_{FH}(t) + \mathrm{B}\, u_s(t)) \cdot p_s(t) \tag{6a}$$

$$\boldsymbol{y}_{\mathrm{FH}}(t) = C\, x_{\mathrm{FH}}(t) + \mathrm{D}\, u_s(t) \tag{6b}$$

where $p_s(t)$ specifies the beginning and the temporal window of integration

$$p_s(t) = \sum_{n=-\infty}^{+\infty} \mathrm{rect}\left(\frac{t - nT - T/2}{\alpha}\right) \tag{7}$$

In order to proceed with the mathematical analysis of the F&H concept, reconsider the linear system given in (5). A generic time-domain representation referred to any other initial state at time t_0 can be

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stated as

$$\boldsymbol{x}(t) = e^{A(t-t_0)}\boldsymbol{x}(t_0) + \int_{t_0}^{t} e^{A(t-\mu)} B\, u(\mu)\, \mathrm{d}\mu \tag{8a}$$

$$\boldsymbol{y}(t) = C\, x(t) + \mathrm{D}\, u(t) \tag{8b}$$

where e^{At} is the state-transition matrix [25]. This representation is also valid for (6) during the time frame defined in (7). Outside the rectangular window the state vector is kept constant, holding the last integration value. If the system starts at rest, i.e. $\boldsymbol{x}(t_0)=0$ for $t<t_0$ with $t_0=T/2-\alpha/2$ as the starting point of integration, for the first α seconds

$$\boldsymbol{x}(t_0+\alpha) = u_0 \cdot \int_{t_0}^{t_0+\alpha} e^{A(t_0+\alpha-\mu)}\, d\mu\, \mathrm{B} \tag{9}$$

Introducing the change of variable $\beta=\mu-t_0$, the F&H system can be completely described for the first integration cycle as follows

$$\boldsymbol{x}_{\mathrm{FH}}[T] = \boldsymbol{x}(t_0+\alpha) = u_0 \cdot \int_{t_0}^{t} e^{A(\alpha-\mu)} d\beta\, B \tag{10a}$$

$$\boldsymbol{y}_{\mathrm{FH}}[T] = \mathrm{C}\, \boldsymbol{x}_{\mathrm{FH}}[T] + D\, u_1 \tag{10b}$$

This result is the initial condition for the next integration period that starts at t_0+T^+ and halts again at $t_0+T+\alpha$. Reiterating from (8), with initial condition $\boldsymbol{x}(t_0+T)=\boldsymbol{x}_{\mathrm{FH}}[T]$ and following the same procedure along time, it can easily be proved (Appendix A) that the states of the F&H system and output are represented by

$$\boldsymbol{x}_{\mathrm{FH}}[nT] = \sum_{i=0}^{n-1} \left(e^{A\,\alpha}\right)^{n-i-1} \cdot \int_0^{\alpha} e^{A(\alpha-\beta)} d\beta\, B \tag{11a}$$

$$\boldsymbol{y}_{\mathrm{FH}}[nT] = \mathrm{C}\, \boldsymbol{x}_{\mathrm{FH}}[nT] + D\, u_n \tag{11b}$$

with $\boldsymbol{x}_{\mathrm{FH}}[nT]=0$ for $n\leq 0$. The output of the system can be formulated as a discrete-time domain signal as follows

$$\boldsymbol{y}_{\mathrm{FH}}[n] = C \cdot \sum_{i=0}^{n-1} u_i \left(e^{A\,\alpha}\right)^{n-i-1} \cdot \int_0^{\alpha} e^{A(\alpha-\beta)} d\beta\, B + D\, u_n \tag{12}$$

Now consider a second system with the same sampled input $u_s(t)$ but represented by

$$\dot{\boldsymbol{w}}(t) = k\, A\, \boldsymbol{w}(t) + k\, \boldsymbol{B}\, u_s(t) \tag{13a}$$

$$\boldsymbol{r}(t) = C\, \boldsymbol{w}(t) + \mathrm{D}\, u_s(t) \tag{13b}$$

This system is very similar to that described in (5), but differing in the feedback matrix A and input vector B that are scaled by k. Moreover, it is allowed to integrate during the full sampling-and-hold period T.

Repeating the same procedure taken to find (12), the response of this new system can be found to be

$$\boldsymbol{w}[nT] = k \cdot \frac{T}{\alpha} \cdot \sum_{i=0}^{n-1} u_i \left(e^{k\,A\,T}\right)^{n-i-1} \cdot \int_0^{\alpha} \mathrm{e}^{k\,\mathrm{A}\,\frac{T}{\alpha}(\alpha-\beta)} d\beta\, B \tag{14}$$

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If now k is set to α/T then the final solution reduces to

$$\boldsymbol{w}[nT] = \sum_{i=0}^{n-1} u_i \left(e^{A\,\alpha}\right)^{n-i-1} \cdot \int_0^{\alpha} \mathrm{e}^{A(\alpha-\beta)} d\beta\, B \tag{15a}$$

$$\boldsymbol{r}[nT] = \mathrm{C}\, \boldsymbol{w}[nT] + D\, u_n \tag{15b}$$

The output signal in the discrete-time domain can in turn be determined by

$$\boldsymbol{r}[n] = C \cdot \sum_{i=0}^{n-1} u_i \left(e^{A\,\alpha}\right)^{n-i-1} \cdot \int_0^{\alpha} \mathrm{e}^{A(\alpha-\beta)} d\beta\, B + D\, u_n \tag{16}$$

Comparing (15a, 15b) and (16), respectively, with (11a, 11b) and (12), it is possible to conclude that when $k = \alpha/T$

$$\boldsymbol{w}[n] = \boldsymbol{x}_{\mathrm{FH}}[n] \tag{17a}$$

$$\boldsymbol{r}[n] = \boldsymbol{y}_{\mathrm{FH}}[n] \tag{17b}$$

Eqs. (17a) and (17b) state that the outputs of both systems are indistinguishable if sampled every $t = nT$. Thus, the F&H system is an equivalent representation of the system defined in (5). Given $k < 1$, it should be noted, however, that the F&H defined by (11a, 11b) would be utilizing k times smaller time constants. Finally, the difference equation that characterizes the F&H is

$$\boldsymbol{x}_{\mathrm{FH}}[n] = e^{k \cdot A \cdot T} \boldsymbol{x}_{\mathrm{FH}}[n-1] + u_{n-1}\left(e^{k \cdot A \cdot T} - I\right) \cdot A^{-1} \cdot B \tag{18a}$$

$$\boldsymbol{y}_{\mathrm{FH}}[n] = C\, \boldsymbol{x}_{\mathrm{FH}}[n] + D\, u_n \tag{18b}$$

The correspondent z-transform represents a step-invariant filter [27], and is given by

$$\frac{Y(z)}{U(z)} = C \cdot \left(I - z^{-1} \cdot \mathrm{e}^{k \cdot A \cdot T}\right)^{-1} \cdot z^{-1} \cdot \left(e^{k \cdot A \cdot T} - I\right) \cdot \mathrm{A}^{-1} \cdot B + D \tag{19}$$

These qualitative and mathematical results show that the discrete-time F&H is a general closed-form procedure that can be applied to filters of any order. The filter may be low-pass, high-pass, band-pass or band-reject. In formal terms, a general F&H for a staircase discrete-time input, followed by an ideal smoothing filter at the sampled output, can be written as (where Ω is the denormalized frequency)

$$\frac{Y(\Omega)}{U(\Omega)} = \begin{cases} C \cdot (j\Omega \cdot I - k \cdot A)^{-1} \cdot k \cdot B + D, & |\Omega| < \dfrac{\pi}{T} \\ 0, \quad \textit{otherwise} \end{cases} \tag{20}$$

One might ask if any active filter implementation can actually be configured into an F&H system. There is no direct answer to this question. The general rule is to start with a known physical active filter implementation and place switches strategically throughout the circuit, such that the current through capacitors is periodically interrupted. However, for (17a, 17b) to hold, the output $y(t)$ has to be defined at the sampling times nT. In this sense, the capacitor voltage (i.e. the state) has to be available at the output structure, at all times, in order to guarantee the correct sampling. This indicates that some active filter configurations may not meet such requirements. However, a circuit transformation can always be applied to try and find a topology where the states are permanently available at the output. The F&H mapping from $H(s)$ to $H(z)$ is not prone to aliasing. Hence, any filter system can be implemented even for high-pass or band-reject filters.

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3. F&H ACTIVE-FILTERS SIMULATION

Consider the general vector-filter representation in Figure 4. Following the previous discussion, switches were strategically placed to control the current flow. Sample-and-holds are added to generate $u_s(t)$, and to synchronize input/output sampling times. A second non-overlapping clock signal controls the internal switches. The state-space representation of the vector-filter prototype is defined by

$$\dot{\boldsymbol{x}}(t) = \begin{bmatrix} \dot{x}_1(t) \\ \dot{x}_2(t) \end{bmatrix} = \rho \begin{bmatrix} -\gamma & 1 \\ -1 & 0 \end{bmatrix} \cdot \begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix} + \begin{bmatrix} \rho \\ 0 \end{bmatrix} \cdot u(t) \tag{21}$$

$$\boldsymbol{y}(t) = \begin{bmatrix} y_{\mathrm{LP}}(t) \\ y_{\mathrm{BP}}(t) \\ y_{\mathrm{HP}}(t) \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ 1 & 0 \\ \gamma & -1 \end{bmatrix} \cdot \begin{bmatrix} x_1(t) \\ x_2(t) \end{bmatrix} - \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix} \cdot u(t) \tag{22}$$

with $\gamma = 3R/(r+R)$ and $\rho = 1/(RC)$. The resulting transition matrix for the F&H system is

$$e^{A \cdot \alpha} = \begin{bmatrix} f_{1,1} & f_{1,2} \\ f_{2,1} & f_{2,2} \end{bmatrix} \cdot \mathrm{e}^{-\gamma \cdot \rho \cdot \alpha/2} \tag{23}$$

where

$$f_{1,1} = \cos\left(\rho \cdot \alpha \cdot \sqrt{1 - \frac{1}{4}\gamma^2}\right) - \frac{\gamma}{\sqrt{4 - \gamma^2}} \cdot \sin\left(\rho \cdot \alpha \cdot \sqrt{1 - \frac{1}{4}\gamma^2}\right) \tag{24}$$

$$f_{1,2} = \frac{2}{\sqrt{4 - \gamma^2}} \cdot \sin\left(\rho \cdot \alpha \cdot \sqrt{1 - \frac{1}{4}\gamma^2}\right) \tag{25}$$

$$f_{2,1} = -_{f1,2} \tag{26}$$

$$f_{2,2} = f_{1,1} + \gamma \cdot \mathrm{f}_{1,2} \tag{27}$$

with $\alpha = k \cdot T$. Table I summarizes the parameter set used to simulate the F&H vector filter. In addition, a continuous-time prototype is also considered for comparison. It uses the same parameter set, except for the capacitor values that are scaled accordingly to $1/k$, being k the duty-cycle of the second-phase clock.

To test the generic discrete-time F&H representation defined by (11) or (12), a simulation was performed with Matlab and confirmed with an electrical simulator. Figure 5 shows the simulation

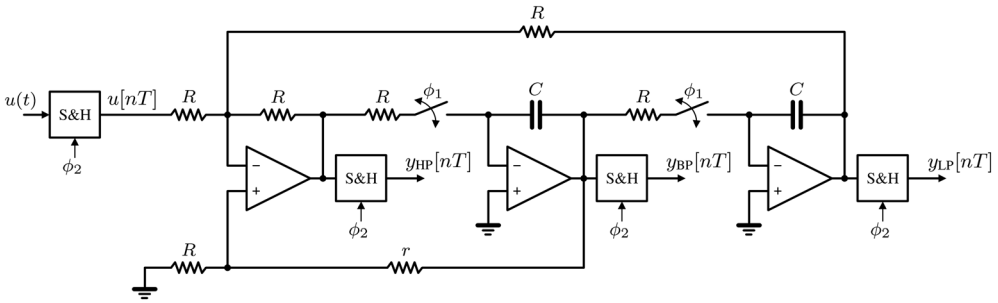

Figure 4. General vector filter with F&H implementation.

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results for the different filter outputs depicted in Figure 4, for both the continuous-time filter (with $1/k$ times bigger capacitors — C-T) and the F&H counterpart (F&H). The input signal bandwidth is $\pi/5$ in normalized frequency ($f_s = 1/3$ MHz). Each plot shows both results for the F&H and the continuous-time scaled version. The input signal utilized for testing is the following band-limited signal

$$u(t) = \sum_{k=0}^{2} \frac{-1}{10^k} \sin\left(2\pi \cdot 10^{k-3} f_s \cdot \mathrm{t}\right) \tag{28}$$

As expected, both F&H and sampled continuous-time system outputs coincide. It can also be verified, in zoomed areas that the non-sampled continuous-time output passes through the points defined at $t = nT$, with the same magnitude as the F&H. This is in agreement with the earlier theoretical developments.

4. EXPERIMENTAL RESULTS

To demonstrate the F&H concept, a prototype was designed for the vector-filter depicted in Figure 4. The discrete implementation of the proposed filter is shown in Figure 6. Four S&H circuits HA5330 with trimmers for offset adjustment from Intersil are employed, one at the input and the remaining at each filtered output. The design comprises rail-to-rail operational amplifiers LMP2011 (1N1A) from National Semiconductor. An ALD1103 IC from Analog Linear Devices is used to implement the required switches, which includes both nMOS and pMOS devices. Transmission-gate configuration is chosen to improve switching operation, at the expense of increased parasitic capacitance. To compare the circuit measurements, an ideal vector-filter was simulated using periodic-ac analysis from Cadence Spectre-RF. In the simulation setup, to account for parasitic capacitances introduced by the discrete devices, a minimum capacitance of 16 pF was added at each node of the schematic.

For the experimental realization, the clock signals were generated with an FPGA Xilinx Virtex-II Pro. The FPGA internal clock is used to obtain the sampling frequency of 333.3 kHz. Non-overlapping clock signals are applied with duty-cycles ranging from 10 to 100%. A different clock signal was generated to drive the S&H independently, preventing the sampling from interfering with switching operation—similarly to the signal scheme illustrated in Figure 2.

Figure 7 shows both measurement and simulation results for the proposed vector filter. The magnitude $|V_{out}/V_{in}|$ is plotted for the three outputs against the frequency range, up to nearly half the sampling rate. As shown, the circuit measurements validate the theoretical developments and attest the realization of the F&H technique.

5. CONCLUSION

The F&H technique has been addressed in this paper, which consists on a sampled-data technique that uses time gating as a multiplication factor to scale time-constants. In more specific terms, it is a mixed analog/discrete-time design approach that combines analog continuous-time conventional filtering with

Table I. Vector filter parameters.

	C-T vector filter	F&H vector filter
R	10 kΩ	10 kΩ
r	82 kΩ	82 kΩ
C	10 nF	1.0 nF
$k = \alpha/T$	–	0.1
$f_0^{(a)} = 1/(2\pi RC)$	1592 Hz	⇔ 1592 Hz
$Q^{(b)} = \frac{1}{3}\left(1 + \frac{r}{R}\right)$	3.1	3.1

[a]Natural frequency.
[b]Quality factor.

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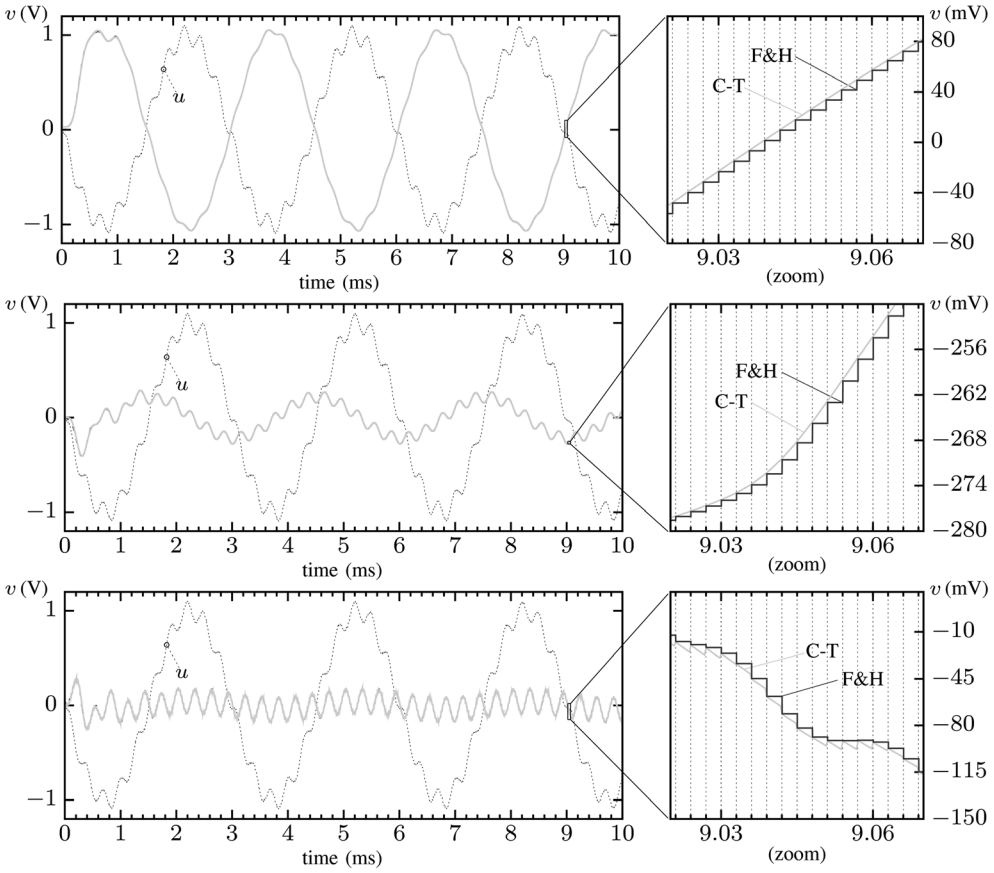

Figure 5. Time response of the F&H and continuous-time (C-T) vector filters for (a) low-pass, (b) band-pass and (c) high-pass outputs.

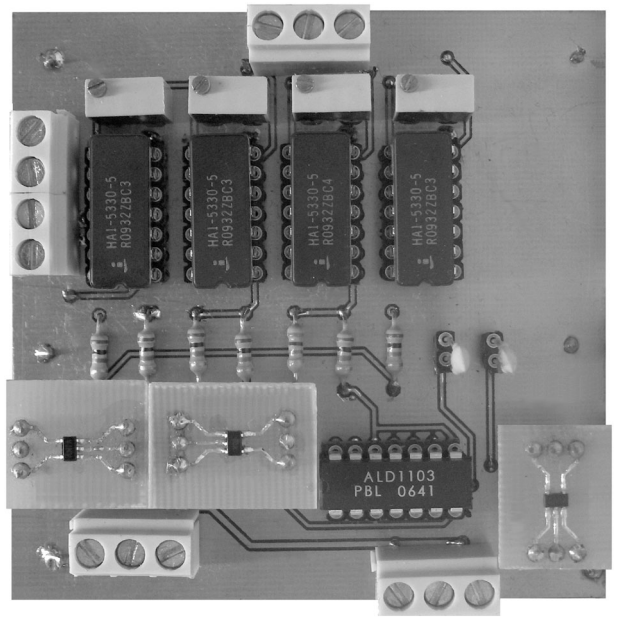

Figure 6. Photograph of the vector-filter prototype implementation.

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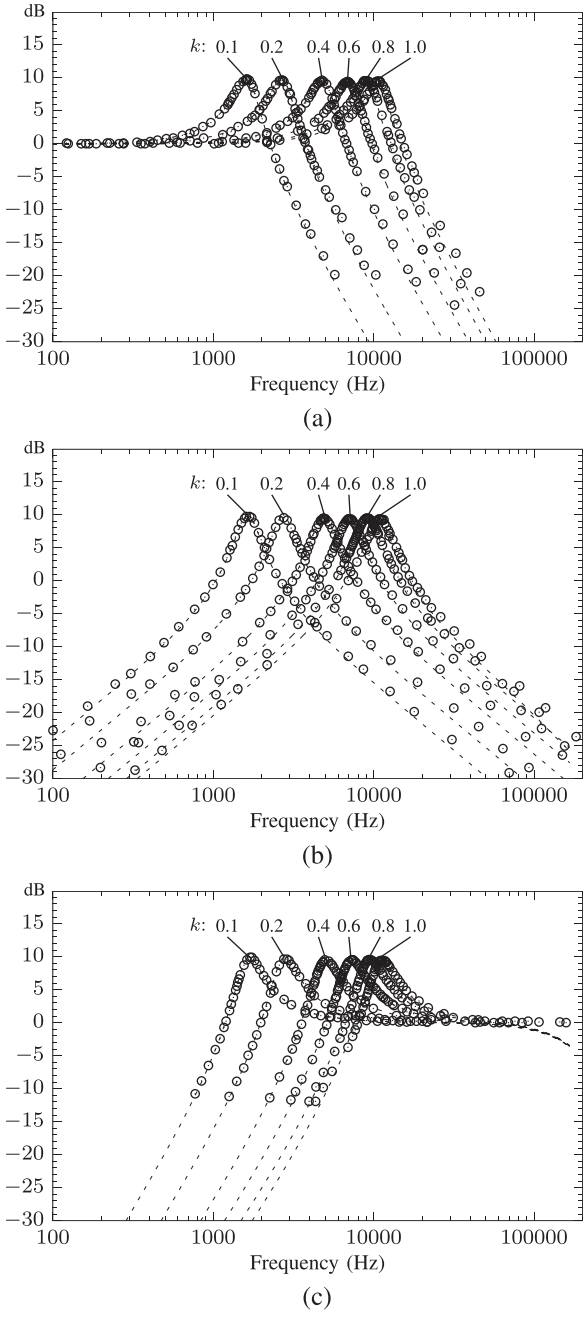

Figure 7. Vector-filter ac magnitude measurements (circles) and simulation results (dashed lines) with different duty-cycles for (a) low-pass, (b) band-pass, and (c) high-pass outputs.

sampling. It offers the possibility of a fully digital tuning procedure, through a PWM-like control over the duty-cycle. The concept of generalization has been derived for sample-and-hold type of input signals. This is not, however, a real limitation in modern systems since, in general, signals are eventually digitally converted and sample-and-hold signals are needed for the analog-to-digital conversion. In fact, this sampling is only needed at the input because the output is inherently of sample-and-hold type. There is no limitation on the poles and zeros location of the original system. The smooth F&H response equals the response of the original system up to $f_s/2$, with poles and zeros locations scaled by the duty-cycle. Experimental results further demonstrated the theoretical derivations and simulation.

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APPENDIX A

If (11) is valid for all n, then for $n+1$ the following set of equations must also hold

$$\boldsymbol{x}_{\mathrm{FH}}[(n+1)T] = \sum_{i=0}^{n} u_i \left(e^{A\,\alpha}\right)^{n-i} \cdot \int_0^{\alpha} e^{A(\alpha-\beta)} d\beta\, B \tag{A.1a}$$

$$\boldsymbol{y}_{\mathrm{FH}}[(n+1)T] = C\,\boldsymbol{x}_{\mathrm{FH}}[(n+1)T] + D\,u_{n+1} \tag{A.1b}$$

with $\boldsymbol{x}_{\mathrm{FH}}[nT]=0$ for $n \le 0$.

The first element of the series is when $n=1$. Then, directly from (11)

$$\boldsymbol{x}_{\mathrm{FH}}[T] = u_0 \cdot \int_0^{\alpha} e^{A(\alpha-\beta)} d\beta\, B \tag{A.2a}$$

$$\boldsymbol{y}_{\mathrm{FH}}[T] = C\,\boldsymbol{x}_{\mathrm{FH}}[T] + D\,u_1 \tag{A.2b}$$

which equals (10). Therefore (11) gives a correct result for the first element of the series. To prove for $n+1$, (11) needs to be calculated using the initial condition $\boldsymbol{x}(t_0+nT-T+\alpha)=\boldsymbol{x}_{\mathrm{FH}}[nT]$ in (8) as follows

$$\boldsymbol{x}_{\mathrm{FH}}[(n+1)T] = \int_{t_0+nT}^{t_0+nT+\alpha} e^{A(t_0+nT+\alpha-\mu)} \cdot B \cdot u_s(\mu)\, \mathrm{d}\mu + e^{A\,\alpha} \sum_{i=0}^{n-1} u_i \left(e^{A\,\alpha}\right)^{n-i-1} \int_0^{\alpha} e^{A\,(\alpha-\beta)} d\beta\, B \tag{A.3}$$

Making the change of variable $\beta=\mu-t_0-nT$ on the first integral and knowing that $u_s(\mu)=u_n$, $\mu \in [t_0+nT, t_0+nT+\alpha]$ then (A.3) results into

$$\boldsymbol{x}_{\mathrm{FH}}[(n+1)T] = \left(\sum_{i=0}^{n-1} u_i \left(e^{A\,\alpha}\right)^{n-i-1} + u_n \right) \cdot \int_0^{\alpha} e^{A\,(\alpha-\beta)} d\beta\, B \tag{A.4}$$

which leads to (A.1) with basic manipulation. Having in mind that the integration is halted for $t \in [nT+\alpha, (n+1)T[$, $n \in \mathbb{N}$, then (A.4) can be represented by (A.1). Therefore, it is demonstrated that (12) represents (6) for all n.

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