InGaZnO Thin-Film-Transistor-Based Four-Quadrant High-Gain Analog Multiplier on Glass

Pydi Ganga Bahubalindruni, Vítor Grade Tavares, Jérôme Borme, Pedro Guedes de Oliveira, Rodrigo Martins, Elvira Fortunato, and Pedro Barquinha

***Abstract*— This letter presents a novel high-gain four-quadrant analog multiplier using only n-type enhancement indium–gallium–zinc-oxide thin-film-transistors. The proposed circuit improves the gain by using an active load with positive feedback. A Gilbert cell with a diode-connected load is also presented for comparison purposes. Both circuits were fabricated on glass at low temperature (200 °C) and were successfully characterized at room temperature under normal ambient conditions, with a power supply of 15 V and 4-pF capacitive load. The novel circuit has shown a gain improvement of 7.2 dB over the Gilbert cell with the diode-connected load. Static linearity response, total harmonic distortion, frequency response, and power consumption are reported. This circuit is an important signal processing building block in large-area sensing and readout systems, specially if data communication is involved.**

***Index Terms*— Multipliers, a-IGZO TFT, positive feedback.**

I. Introduction

IGZO TFT technology allows low-cost flexible and/or transparent large-area electronics, which can find potential applications in various fields besides display technology, such as in biomedical [1]. Therefore, analog mixed-signal circuit design with this technology is gaining significant interest. Up to now, analog design has been mostly focused on amplifiers [2], [3] and data converters [4]. However, multipliers are important functional blocks for signal processing operation. They find promising application in large-area sensing systems, specially when the readout circuits response needs to be modulated for communication and interfacing [5]. Nonetheless, the work done towards the mixer or multiplier implementation with oxide TFTs is very limited [6]. In this letter a high-gain novel analog multiplier based on differential Gilbert cell [7] is characterized from measurements and, to the authors best knowledge, for the first time.

Unavailability of reproducible p-type oxide TFTs is one of the technology limitations that restricts the design of high-gain topologies. However, this limitation can be addressed with circuit design techniques, such as active load with cascode bootstrapping [2] and positive feedback [8].

The work starts with the characterization of a Gilbert topology using a diode connected transistor as the load (referred as 'Mul1'). Since there are no benchmarks for the multiplier performance in the literature with oxide TFT technology, Mul1 is used as a reference to assess the perfomance of the proposed circuit, referred from here on as 'Mul2'. Its high gain is achieved with an active load employing positive feedback [8]. Both circuits were implemented solely with n-type enhancement TFTs in order to minimize the number of needed masks, processing steps and hence the fabrication cost.

An in-house model was used for circuit simulations [9], and the corresponding integrated circuit (IC) fabrication took place at room temperature, followed by annealing at 200°C. The fabrication process is the same as described in [9], except that sputtered Mo is now used for drain, source, gate electrodes and interconnections in the circuit layout. Devices show a turn on voltage of −0.9 V, a threshold voltage of 0.85 V, a mobility of 20 cm^2/V.s, and a subthreshold slope of 0.2 V/dec.

A. Gilbert Cell With Diode Connected Load (Mul1)

The circuit schematic and micrograph are shown in Fig. 1a and 1b, respectively. Mul1 is implemented with three differential pairs (T1-T2, T3-T4 and T5-T6), with T0 representing the biasing transistor. Both T7 and T8 are diode connected transistors, acting as active loads with an impedance of $1/g_{m7,8}$.

For analysis purposes, the I/V relationship for TFTs is roughly approximated by the well known 'level1' FET expression. Having all transistors in saturation, the drain current is then represented by,

$$i_{DS} \approx \tfrac{1}{2} K (v_{GS} - V_{TH})^2. \quad (1)$$

After few manipulations, the differential output current (i_{OUT}) and the voltage (v_{OUT}) of the multiplier for small differential

Manuscript received December 24, 2015; revised February 8, 2016; accepted February 22, 2016. Date of publication February 29, 2016; date of current version March 22, 2016. This work was supported in part by the FEDER funds through the COMPETE 2020 Programme and National Funds through FCT - Portuguese Foundation for Science and Technology under Project CMUPT/SIA/0005/2009, Project UID/CTM/50025/2013, and Project EXCL/CTM-NAN/0201/2012, in part by the European Communities 7th Framework Programme under Grant ICT-2013-10-611070 (i-FLEXIS project), and in part by the H2020 program under Grant ICT-03-2014-644631 (ROLL-OUT project). The review of this letter was arranged by Editor W. S. Wong.

P. G. Bahubalindruni, R. Martins, E. Fortunato, and P. Barquinha are with i3N/CENIMAT, Department of Materials Science, Faculty of Science and Technology, Universidade NOVA de Lisboa and CEMOP/UNINOVA, Campus de Caparica, 2829-516 Caparica, Portugal (e-mail: p.bahubalindruni@campus.fct.unl.pt).

V. G. Tavares and P. G. de Oliveira are with the Faculty of Engineering, Instituto de Engenharia de Sistemas e Computadores, Tecnologia e Ciência, University of Porto, Porto 4200-465, Portugal.

J. Borme is with the International Iberian Nanotechnology Laboratory, Braga 4715-330, Portugal.

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/LED.2016.2535469

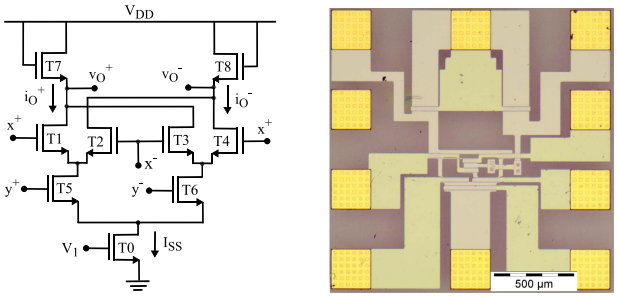

Fig. 1. Mul1. (a) Circuit schematic. (b) Micrograph.

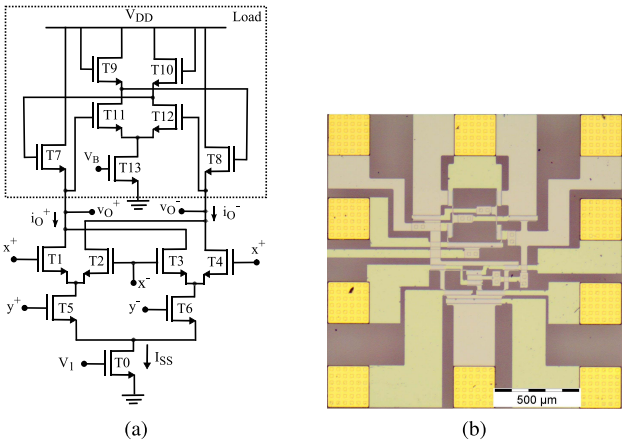

Fig. 2. Mul2. (a) Circuit schematic. (b) Micrograph.

input voltages x and y are given by,

$$i_{\mathrm{OUT}} = i_{\mathrm{O}}^{+} - i_{\mathrm{O}}^{-} \approx Kxy$$
$$v_{\mathrm{OUT}} = v_{\mathrm{O}}^{+} - v_{\mathrm{O}}^{-} = \frac{1}{g_{m7,8}}(i_{\mathrm{OUT}}) \propto xy. \tag{2}$$

B. High-Gain Gilbert Cell (Mul2)

The circuit schematic and micrograph of the fabricated circuit are shown in Fig. 2. Higher gain can be achieved with Mul2 when compared to Mul1, by forcing the same signal level at both gate and source terminals of load transistors (T7 and T8). This goal can be resolved with the help of positive feedback, which is accomplished by T9 to T13 in Fig. 2a.

It should be noted that v_{O}^{+} and v_{O}^{-} are 180^{o} out of phase, but, because of the cross-connection operated by the differential pair T9-T13, the gate voltages of T7 and T8 become in phase with v_{O}^{+} and v_{O}^{-}, respectively. Thus, a simplified representation of the load and its small signal model can be represented as shown in Fig. 3. The positive feedback gain (A_f) is controlled by the feedback network formed by the TFTs (T9 to T13) and can be expressed by,

$$A_f = \frac{g_{m11,12}}{g_{m9,10} + g_{ds9,10} + g_{ds11,12}}. \tag{3}$$

From Fig. 3b, the load resistance formed by T7 or T8 are given by,

$$\frac{v_o}{i_o} = \frac{1}{g_{m7,8}(1 - A_f) + \frac{1}{r_{o7,8}}}. \tag{4}$$

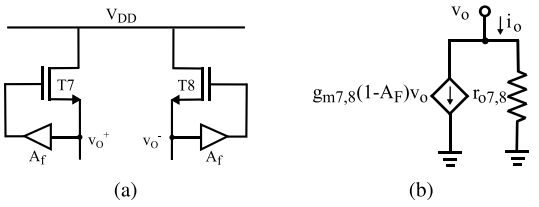

Fig. 3. Mul2 load. (a) Simplified equivalent. (b) Small signal model.

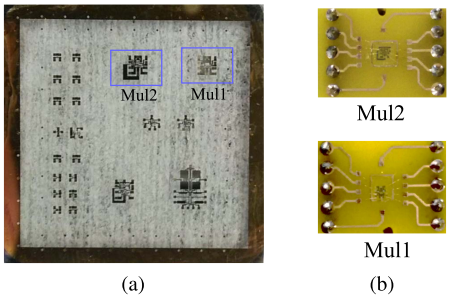

Fig. 4. (a) Glass substrate containing the circuits and isolated TFTs. (b) Mul1 and Mul2 after dicing and wire-bonding.

By making the A_f close to unity, a very high signal-equivalent impedance ($r_{o7,8}$) can be achieved. However, care needs to be taken concerning the feedback strength. If A_f is too high, then the effective load resistance may become negative, which causes stability problems. Therefore, to ensure stable operation A_f must be less than or equal to unity. Mul2 output voltage is given by,

$$v_{\mathrm{OUT}} = \frac{1}{g_{m7,8}(1 - A_f) + \frac{1}{r_{o7,8}}}(i_{\mathrm{OUT}}). \tag{5}$$

Under the same biasing conditions Mul2 and Mul1 gains can be related by,

$$\frac{(A_V)_{Mul2}}{(A_V)_{Mul1}} = \frac{g_{m7,8}}{g_{m7,8}(1 - A_f) + \frac{1}{r_{o7,8}}}. \tag{6}$$

showing that the gain improvement can be as much as the intrinsic gain of the transistor as A_f reaches unity.

II. Results and Discussion

A. Circuits Preparation for Measurements and Test Setup

Both circuits were fabricated on the same glass substrate, as shown in Fig. 4, and subjected to the same processing conditions in order to provide a fair comparison. Prior to dicing and wire-bonding of individual samples, photoresist was deposited on the entire substrate with spin-coating, in order to protect the circuits from the glass particles that scatter during dicing. Later, the isolated circuits were cleaned with acetone, isopropanol, distilled water and dried with nitrogen. Wire-bonding (with aluminum) was performed between the circuit contacts (Mo) and the printed circuit board tracks (silver). Both circuits were tested under normal ambient conditions. Two linearity assessments were made, a static evaluation and another via the determination of total harmonic distortion (THD). The characterization of the static linearity response was performed with the help of a digital multimeter (Proteck 506). On the other hand, during THD

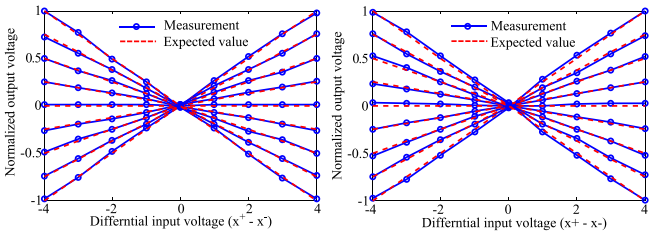

Fig. 5. Linearity response and validation with expected value in the normalized form (a) Mul1, (b) Mul2.

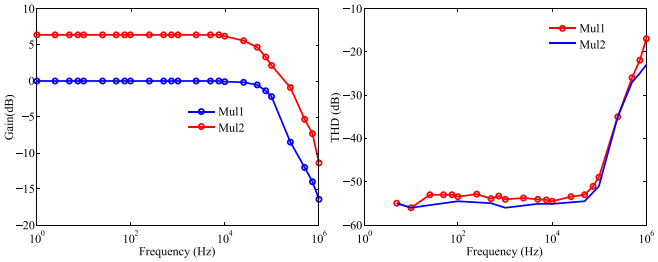

Fig. 6. (a) Frequency response. (b) THD.

TABLE I
MUL1 AND MUL2 COMPARISON

Circuit	No. of TFTs	Power (mW)	Linearity error (%)	gain (dB)	Bandwidth (kHz)
Mul1	9	0.9	9	0	150
Mul2	14	1.1	11	7.2	85

and frequency response characterization, a unity gain buffer (implemented with external IC) was used, which shows approximately 4 pF capacitive load to the circuits under test. For these measurements, an AFG3021B single channel arbitrary function generator and a DS2024B four channel digital storage oscilloscope were used.

The devices in Fig. 1 and 2 were set with the following sizes: $W_{T0} = 320\ \mu m$, $W_{(T1\text{-}T4)} = 80\ \mu m$, $W_{(T5\text{-}T8)} = 160\ \mu m$. In Fig. 2, $W_{T13} = 320\ \mu m$, $W_{(T11\text{-}T12)} = 70\ \mu m$ and $W_{(T9\text{-}T10)} = 80\ \mu m$. All TFTs present a total gate to source and gate to drain overlap of $10\,\mu m$. Considering the order of magnitude of the overlapping, a minimum channel length of $20\,\mu m$ was set. As it can be noticed, bigger TFT dimensions were employed in the differential pair in order to minimize mismatches and the consequent offsets. In addition, the dimensions of the TFTs in the Mul2 feedback network were chosen to ensure $A_f < 1$. The power supply is set to 15 V in all experiments. The measured static linearity response of both circuits are confronted with the expected ideal results in the normalized form, as shown in Fig. 5, and for the following stimulus (by keeping all the TFTs in saturation),

$$x = 8 \pm 2V, \quad y = 5 \pm 2V, \quad V_1 = 1.9V, \quad V_b = 1.75V. \quad (7)$$

The performance metrics are summarized in Table I. They show that Mul2 presents a slightly higher non-linearity for the same input level in comparison to Mul1. Here it should be noted that the Mul2 output swing is much higher compared to Mul1. Circuit simulations also reveal that if the input level is kept constant the worst case linearity error increases with respect to A_f. The outcome suggests that as close as the impedance reaches r_o, higher non-linearity will result because of higher output voltage level.

The frequency response and THD are presented in Fig. 6. For this experiment, one of the inputs was set to a small dc voltage (0.5 V), while the other was connected to a sin signal. As expected, Mul2 shows a higher gain. The 7.2 dB gain improvement is a result of a fairly conservative A_f to guarantee stability. On the other hand, both circuits are showing similar THD for similar output signal levels. Table I also reveals that Mul2 has higher power consumption, which is due to the additional current provided by the bias transistor (T13) in Fig. 2a.

III. CONCLUSION

For the first time, an analog multiplier or mixer is characterized with the oxide TFT technology using only n-type enhancement type devices. A high-gain multiplier is proposed, characterized and compared with the traditional Gilbert cell with diode connected load. The gain of the proposed circuit can be controlled and increased further by making the feedback gain (A_f) closer to unity.

REFERENCES

[1] M. Takamiya, H. Fuketa, K. Ishida, T. Yokota, T. Sekitani, T. Someya, and T. Sakurai, "Flexible, large-area, and distributed organic electronics closely contacted with skin for healthcare applications," in *Proc. Int. Midwest Symp. Circuits Syst. (MWSCAS)*, Aug. 2014, pp. 829–832, doi: 10.1109/MWSCAS.2014.6908543.

[2] P. G. Bahubalindruni, B. Silva, V. G. Tavares, P. Barquinha, N. Cardoso, P. G. de Oliveira, R. Martins, and E. Fortunato, "Analog circuits with high-gain topologies using a-GIZO TFTs on glass," *J. Display Technol.*, vol. 11, no. 6, pp. 547–553, Jun. 2015, doi: 10.1109/JDT.2014.2378058.

[3] K. Ishida, R. Shabanpour, B. K. Boroujeni, T. Meister, C. Carta, F. Ellinger, L. Petti, N. S. Münzenrieder, G. A. Salvatore, and G. Tröster, "22.5 dB open-loop gain, 31 kHz GBW pseudo-CMOS based operational amplifier with a-IGZO TFTs on a flexible film," in *Proc. Asian Solid-State Circuits Conf. (A-SSCC)*, Nov. 2014, pp. 313–316, doi: 10.1109/ASSCC.2014.7008923.

[4] D. Raiteri, F. Torricelli, K. Myny, M. Nag, B. Van der Putten, E. Smits, S. Steudel, K. Tempelaars, A. Tripathi, G. Gelinck, A. Van Roermund, and E. Cantatore, "A 6 b 10 MS/s current-steering DAC manufactured with amorphous gallium-indium-zinc-oxide TFTs achieving SFDR > 30 dB up to 300 kHz," in *Proc. Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2012, pp. 314–316, doi: 10.1109/ISSCC.2012.6177028.

[5] Y. Hu, L. Huang, W. S. A. Rieutort-Louis, J. Sanz-Robinson, J. C. Sturm, S. Wagner, and N. Verma, "A self-powered system for large-scale strain sensing by combining CMOS ICs with large-area electronics," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 838–850, Apr. 2014, doi: 10.1109/JSSC.2013.2294326.

[6] G. Bahubalindruni, C. Duarte, V. G. Tavares, P. Barquinha, R. Martins, E. Fortunato, and P. G. de Oliveira, "Multipliers with transparent a-GIZO TFTs using a neural model," in *Proc. 20th Telecommun. Forum (TELFOR)*, Nov. 2012, pp. 955–958, doi: 10.1109/TELFOR.2012.6419367.

[7] J. N. Babanezhad and G. C. Temes, "A 20-V four-quadrant CMOS analog multiplier," *IEEE J. Solid-State Circuits*, vol. 20, no. 6, pp. 1158–1168, Dec. 1985, doi: 10.1109/JSSC.1985.1052454.

[8] P. U. Calzolari, G. Masetti, and M. Severi, "Integrated n.m.o.s. operational amplifier for c.c.d. transversal filters," *Electron. Lett.*, vol. 15, no. 1, pp. 29–31, Jan. 1979, doi: 10.1049/el:19790022.

[9] P. Bahubalindruni, V. G. Tavares, P. Barquinha, C. Duarte, P. G. de Oliveira, R. P. Martins, and E. Fortunato, "Transparent current mirrors with a-GIZO TFTs: Neural modeling, simulation and fabrication," *J. Display Technol.*, vol. 9, no. 12, pp. 1001–1006, Dec. 2013, doi: 10.1109/JDT.2013.2275251.